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A new electrode structure of IrO_x/Bi-doped $SrRuO_3$ for highly reliable La-doped Pb (Zr, Ti)O_3-based ferroelectric memories

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Abstract— **We successfully developed a lanthanum (La)-doped Pb (Zr,Ti)O_3 (PLZT) based ferroelectric capacitor (FC) using a new electrode material of bismuth (Bi) doped $SrRuO_3$ (B-SRO) aiming at reduction of energy consumption of ferroelectric random access memory (FeRAM) by suppressing the leakage current of its FC. Our employed B-SRO layer is effective for suppressing the leakage current due to reducing atomic interdiffusions of Iridium and lead between IrO_x top electrode (TE) and PLZT. Space charge limited conduction (SCLC) is dominant in the leakage current of the FC with B-SRO, while defect assisted conduction possibly includes in the leakage current of FC without B-SRO in addition with the SCLC. Switchable polarization, depending on the B-SRO thickness, has largest value for 1.0-1.5 nm thick B-SRO. Excellent imprint and switching (fatigue) endurances is proven on the FC with 1 nm thick B-SRO.**

Keywords- component; ferroelectric memory; FRAM; FeRAM; Bi doped $SrRuO_3$

I. INTRODUCTION

Ferroelectric random access memory (FeRAM or FRAM), a type of non-volatile memory using ferroelectric materials, has excellent electric properties, such as high switching (fatigue) endurance and high writing speed [1-5], Thus FeRAM is suitable for the applications of edge devices used in internet environments, such as Internet of things (IoT). However, FeRAM needs to further lower energy consumption by suppressing leakage current of the ferroelectric capacitor (FC) and to further improve in reliability including rewriting endurance (fatigue endurance) and memory storage stability for commercializing stand-alone FeRAM with large memory density [6] and embedded FeRAM [7,8] in the system on chip (SOC). Embedded FeRAM is often employed for the edge devices, where FC is not only used in the memory storage but also used in the peripheral capacitor aiming for dye (chip)-size shrinkage. Thus, FC in the embedded FRAM needs to reduce the leakage current to minimize the total energy consumption in the SOC. HfO_2 and its related ferroelectric materials (HfO_2-FE) have recently attracted much attention because HfO_2-FE appears to be fully compatible with CMOS fabrication due to its low growth temperature [9-13].

It has been reported that HfO_2-FE achieved remarkable electric properties including low leakage current for even a few nm-thick HfO_2-FE and memory storage stability up to 10 years, and fatigue endurance of more than 10^{10} cycles [13,14], However, enough evidence regarding the reliability for realizing commercially available FeRAM using HfO_2-FE has been gathered yet. For example, time-dependent dielectric breakdown (TDDB) has been serious problem since 10 nm or thinner HfO_2-FE needs to be used for low voltage operation because of its large coercive field close to electric break down electric field [15,16].

Therefore, we have employed sputter-deposited lanthanum-doped $Pb(Zr_{0.4},Ti_{0.6})O_3$ (PLZT), which has accumulated enough reliable data over about two decades since PLZT based FeRAM was commercialized. Although metal organic chemical vapor deposition (MOCVD)-based $Pb(Zr,Ti)O_3$ (PZT) has achieved excellent electric properties of a low voltage saturation polarization [17-20], the production cost of sputter deposited PLZT is lower than that of MOCVD PZT. We have reported that our developed FC consisting of two PLZT stacked layers and two IrO_x ($1<x<2$) stacked top electrodes (TE) revealed excellent electric properties of a low voltage operation and high reliability at temperatures from -45℃ to 125℃ [21]. However, leakage current of our developed FC was found to be too large to

apply to the large memory density FeRAM and the embedded FeRAM. Since the control of the interface between the TE and PLZT is crucial to obtain good electronic properties of FC in our experiment [22, 23], we sought to improve the leakage current of PLZT-based FCs employing a $SrRuO_3$ (SRO) film for an interlayer between IrO_x TE and PLZT. However, although SRO has been well investigated as an interlayer material between metal electrode and perovskite ferroelectric materials to improve electric properties [24-27], the film quality of the sputter-deposited SRO is not so good because density of SRO target is up to 85%. Cross et al. reported the FC with SRO interlayer revealed large leakage current because of large Sr interdiffusion [27], which is considered that SRO was easily decomposed and induced the interdiffusion between SRO and PZT (PLZT) resulting in large leakage current [24]. We have improved FC characteristics applying Bi-doped SRO (B-SRO) as an interlayer which was sputter-deposited using newly developed B-SRO target whose atomic density can be increased up to 95%.

In this paper, we describe the fabrication of our developed FC and its electrical characteristics, focusing on the leakage current, polarization by varying B-SRO thickness, and making sure the reliability of the B-SRO FC. Finally, we discuss the cause of its good electrical performance.

II. Experimental methods

Since we found that {111} crystalline orientation of our sputter deposited PLZT on a {111} oriented Pt is the most preferable to obtain a good FC performance among other orientations [28], we fabricated a PLZT-based FC, consisting of a {111} crystalline oriented Pt bottom electrode, a {111} crystalline oriented PLZT layer, and a IrO_x TE layer, by using 180-nm node CMOS manufacturing technology. The PLZT layer and the IrO_x TE consisted of a stacked structure for improving electric characteristics [22]. In this experiment, we tried to applied B-SRO as an interlayer between IrO_x and PLZT. We prepared two types of FC specimens with and without B-SRO, respectively. After Pt and 75 nm thick PLZT layers sequentially deposited at RT on a SiO_2-coated 200 mm-diameter Si wafer, the specimens were annealed by rapid thermal annealing (RTA) at 620℃ in an Ar-based 1.25% O_2 atmosphere for 90 s. A 10 nm-thick PLZT was deposited over the PLZT. Then a B-SRO layer was deposited by varying its thickness from 0.1 nm to 3 nm at 200℃ in 0.5-Pa Argon atmosphere. After B-SRO deposition, a 25 nm-thick IrO_x deposited by sputtering at 300℃ in situ [36]. Then, specimens were annealed by RTA at 725 ℃ in an Ar-based 1.0% O_2 atmosphere for 120 s, and a 150 nm-thick IrO_x was deposited by reactive sputtering at RT. FeRAM arrays were fabricated using our ordinal metallization method [23]. The electric characteristics of the leakage current and the applied voltage dependence of switchable polarization (Q_{sw}) [28] were measured on a 25 × 100 μm^2 square FC. Reliability measurements of imprint test and fatigue test were caried out on the arrayed FC consisting of 2488 FCs (each of 0.80 × 1.35 μm^2 in area) connected in parallel, with a total area of 2687 μm^2 (arrayed FC). In the measurement of leakage current on FC, voltages were applied to BE with grounding bottom electrode (BE). In the measurement of B-SRO thickness dependence of Q_{sw}, we used a 10-μs wide square pulse by varying together with writing and reading voltages from 0 V to 4.0 V; the interval time of reading and writing was 1 s. We investigated the reliability of FeRAM with and without B-SRO by characterizing the imprint and the switching endurance (fatigue) on the arrayed FCs. Imprint is the tendency of stabilizing the stored polarization state mainly due to charged defects existing in the ferroelectric material near the electrode, which degrades the rewriting ability of FeRAM. For manufacturing FeRAM, the imprint test checks the ability of the FC to rewrite the stored data as opposite data (“ opposite state” or OS), for example, writing and storing ‘1 ’ , baking the FC, and then rewriting the stored ‘1’ as ‘0’. In this experiment, we measure the Q_{sw} of an arrayed FC after rewriting of an arrayed FC after baking at 90℃ for imprint acceleration, we call that Q_{sw} as Q_{os} [29]. Fatigue is observed as decrease in polarization of FC from the original during iteration of polarization reversal. In this experiment, we measured the polarization after nth iteration of polarization reversal with 7 V-square pulse at 90℃ on an arrayed FC for fatigue acceleration. The atomic interdiffusion and crystalline structure near the interface between IrO_x/B-SRO and PLZT were investigated via secondary ion mass spectroscopy (SIMS) and transmission electron spectroscopy (TEM). The details are presented elsewhere [21-23, 29-32].

III. Results and Discussion

A. Experimental Results

Figure 1 shows the cross-sectional TEM image of the IrO_x/B-SRO/PLZT interface on the specimen with 1.0 nm thick B-SRO, which clearly reveals that B-SRO layer, as indicated by the red dashed curve in Fig. 1, was almost uniformly deposited on the PLZT layer. Leakage current density (J_{leak}) vs applied voltage (V_{app}) characteristics [33-35] on the FC specimens fabricated by varying B-SRO thickness is shown in Fig. 2. J_{leak} is drastically suppressed by B-SRO and clearly decreased with increasing B-SRO thickness. However, J_{leak} vs V_{app} shapes of all specimens seem to be all similar. Relations between Log J_{leak} and Log V_{app} on the specimens with 1.0 nm-thick B-SRO and without B-SRO by varying measurement temperature from -45℃ to 125℃ are shown in Figs. 3(a) to (d), which shows that the slopes on the specimen with B-SRO are slightly steeper than those on the specimens without B-SRO at the same measurement temperature.

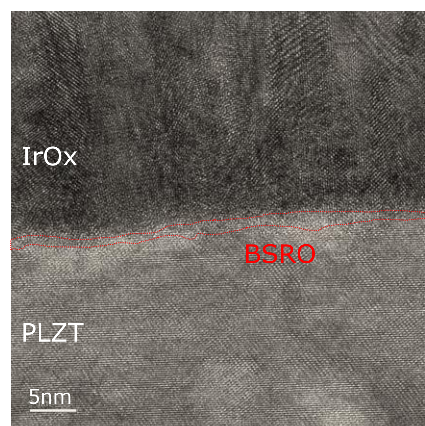

Figure 1. Cross-sectional TEM image of IrO_x/1 nm-thick B-SRO/PLZT interface. The red broken line marks the boundaries B-SRO.

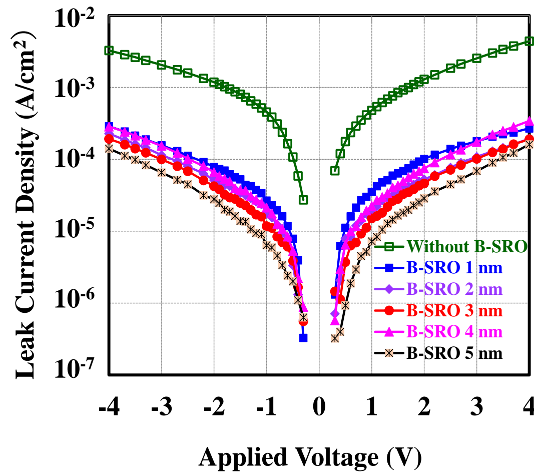

Figure 2. Applied voltage dependence of Leakage current density by varying B-SRO thickness from 0 nm to 5 nm.

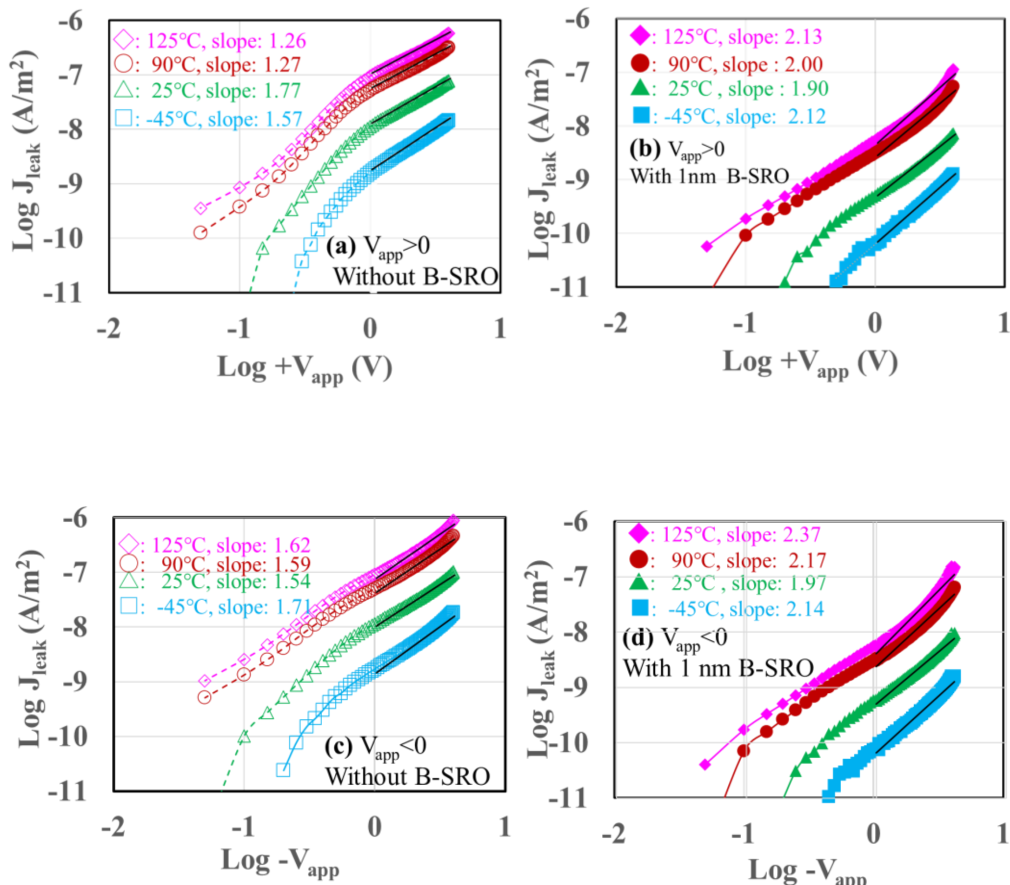

Figure 3. Log J_{leak} (leakage current density) vs Log $+V_{app}$ (applied voltage) (a, b), and Log J_{leak} (leakage current density) vs Log $-V_{app}$ (applied voltage) plots (c, d) of the specimens without B-SRO (a, c), with 1 nm-thick B-SRO (b, d). $+V_{app}$ and $-V_{app}$ indicate positive and negative applied voltages on the top electrode, respectively. Black solid lines indicate fitting lines.

The applied voltage dependence of Q_{sw} by varying the B-SRO thickness from 0 to 5 nm are shown in Fig. 4. The specimen with 1 nm thick B-SRO had the largest Q_{sw}. Our precise investigation revealed that the applied voltage dependency of Q_{sw} with 0.7, 1.0 and 1.3 nm thick B-SRO were almost same.

Baking time dependences of Q_{os} on the specimens fabricated by varying B-SRO thickness from 0 to 5 nm is shown in Fig. 5(a). It was observed that the thinner B-SRO was applied to the specimens, the more rapidly decreased in Q_{os}. Q_3 rate [36], an indicator of decreasing rate in the Q_{os} per unit time derived from the baking time dependences of Q_{os}, is

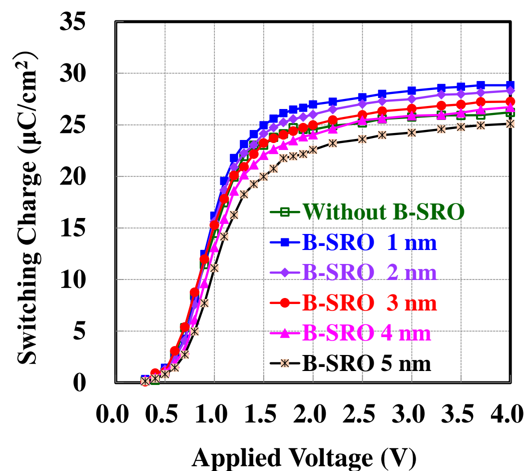

Figure 4. Applied voltage dependence of Q_{sw} on the specimens fabricated by varying the B-SRO thickness every 1 nm from 0 nm to 5 nm.

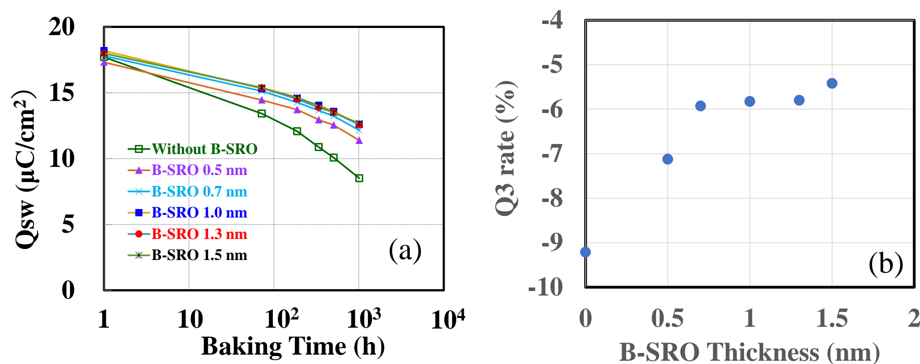

Figure 5. Baking time dependence of Q_{os} on the specimens fabricated by varying B-SRO thickness from 0 nm to 1.5 nm (a) and Q_3 rate (b).

show in Fig. 5(b). Q_3 rate of the specimens with 0.7 nm or thicker SRO are larger than -6%, which is enough value for 10-year guarantee of imprint endurance. Switching cycle dependence of Q_{sw} (fatigue) obtained by stress voltage of 7 V and read voltage of 1.8 V at 90℃ on the specimens fabricated with varying B-SRO thickness are shown in Fig. 6, where each measured Q_{sw} was normalized by the initial Q_{sw}. The thinner B-SRO was applied to the specimen, the weaker fatigue endurance was observed. The stress voltage dependences of Q_{sw} loss in the switching cycle was well described in a power-low model as generally used for the FC fatigue analysis [1, 2, 18]. Considering a simple Arrhenius process [37] for Q_{sw} loss by switching cycles, we can calculate the acceleration ratio for the switching cycles of $4x10^5$ when operating the FeRAM at 125℃ with operating voltage of 1.8 V, for example 10^8 cycles in Fig. 6 being to $4x10^{13}$, which resulted in our 4 Mb FeRAM production [6].

Ir, Pb, O, Sr, and Ru profiles measured by SIMS on the specimens with 1 nm thick B-SRO and without B-SRO are shown in Figs. 7(a) to (e), respectively. Unfortunately, Bi profile was not able to be measured because of some interference by other elements. It was observed that Ir diffusion into PLZT from IrO_x TE on the specimen without B-SRO clearly larger than that on the specimen with B-SRO. It was also observed that Pb diffusion into IrO_x TE from PLZT on the specimen without B-SRO slightly larger than that on the specimen with B-SRO, as indicated by red arrow in Fig. 7(b).

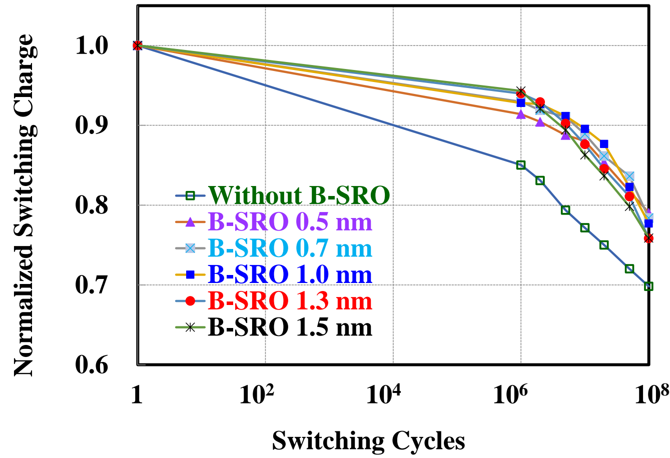

Figure 6. Switching cycle dependence of Q_{sw} (fatigue endurances) on the specimens fabricated by varying B-SRO thickness from 0 nm to 1.5 nm.

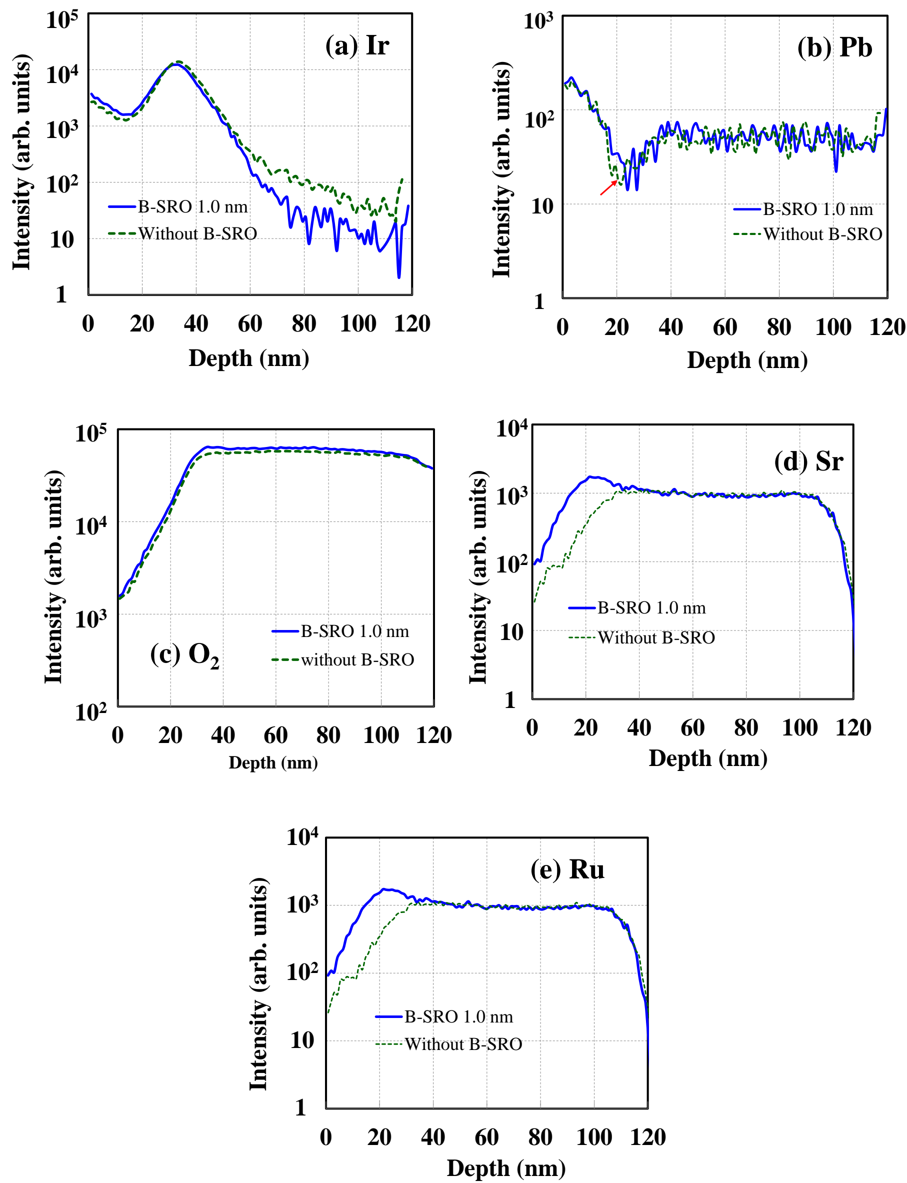

Figure 7. Depth profiles of iridium (a), lead (b), oxygen (c), strontium (d), and ruthenium (e) near the IrO_x/B-SRO/PLZT interface.

B. Discussion

Masuda et al. [38] investigated the leakage current mechanism of their Pt/SRO/PZT capacitor and showed that slope of Log J_{leak} -Log E (electric field) was around 1 in the low field region (<55 kV/cm) and around 2 in the high field region (>55 kV/cm). Although our experimental results are similar to their results, slopes of Log J_{leak}-Log V_{app} curves in our experiment appears to change around 1 V (118 kV/cm). Thus, we evaluated the slopes in the absolute applied voltage 1 V or larger, as indicated by insertions in Figs. 3(a) to (c). Slopes of Log J_{leak}-Log V_{app} on the FCs with B-SRO are almost 2 while slopes of the FCs without B-SRO are around 1.5 in the applied voltage at 1 V or larger, which means that SCLC should be dominant in the leakage current of the FC with B-SRO. In the case of the FC without B-SRO, the leakage current possibly includes other conduction mechanism rather than SCLC. Some preceding studies reported that the FC with an electrode consisting of an SRO layer had large leakage currents [24, 37]. Masuda et al. reported that SRO/PZT did not form Schottky barrier due to interdiffusion between SRO and PZT [37]. Cross et al. also observed large leakage current on the FC with SRO/PLZT because Sr from SRO easily diffused into PLZT, resulting in making leakage pass in the PLZT grain boundaries [24]. In the other hand, Kumura et al. obtained good electric performance on their PZT-based capacitor with IrO_2/SRO TE because SRO can supply oxygen to oxygen deficient region of the PZT and IrO_2 has much less catalytic effect to create hydrogen radical in their FeRAM fabrication process [27]. We consider that our employed B-SRO hardly decompose even in the thin films, which effectively suppress the interdiffusion of Ir and Pb, resulting in reducing the leakage current density on the specimen with B-SRO. It should be noted that the leakage current under 1 V is too low to significantly affect our FeRAM performance. Considering the Ir and Pb interdiffusion on the specimen without B-SRO, Ir impurity or Pb vacancy in the PLZT near IrO_x interface possibly enlarges the leakage current on the specimen without B-SRO. Thus, the values of the fitting-line slope of Log J_{leak} vs Log V_{app}, as show in Fig. 3 (a)-(d), on the specimen without B-SRO is much less than two, in comparison with those /on the specimen with 1 nm thick B-SRO. Although oxygen out-diffusion or interdiffusion possibly influences the electric properties of FC, limited resolution of SIMS in this work did clarify this evidence

It is interested that Q_{sw} depends on the B-SRO thickness. We found that a slight diffusion of Ir from IrO_x TE into PLZT interface enhanced polarization reversal, which eventually enlarged the Q_{sw} of PLZT-based FC in our previous work [23]. Since this effect is sensitive to the amount of diffused Ir, Q_{sw} strongly depends on the B-SRO thickness. In the case of thick B-SRO, Ir diffusion is too low exhibit the effect of polarization reversal. In the case of thin B-SRO, Ir deeply diffused into PLZT resulting in low polarization due to low crystalline quality of PLZT. From our precise experiments, we concluded that B-SRO thickness from 1.0 nm to 1.5 nm should be the most preferable to obtain good performance and reliability of FeRAM. We confirm that much more scalable FeRAM should be manufactured combing the FC with B-SRO and our developed "capacitor over bit line (COB)" technology [39].

IV. Conclusion

We developed a lanthanum-doped $Pb(Zr_{0.4},Ti_{0.6})O_3$ (PLZT)-based ferroelectric capacitor (FC) applying to stand-alone and embedded FeRAMs using Bi-doped $SrRuO_3$ (B-SRO) as an insertion layer between IrO_x top electrode (TE) and PLZT, focusing on suppressing the leakage current. The leakage current was successfully reduced by almost one order of magnitude using B-SRO due to the suppression of Ir and Pb interdiffusion and the largest Q_{sw} was obtained on FC with 1.0-1.3 nm thick B-SRO due to slight diffusion of Ir into PLZT interfaces. Excellent imprint and switching (fatigue) endurances was proven on the FC with 1.0 nm thick B-SRO.

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