Fast carrier recovery in FHSS systems with DDS based Costas loop

Slavko Šajić

Abstract—**Owing to fast change of carrier frequency, the usage of coherent demodulation methods in Frequency-Hopping Spread Spectrum (FHSS) communication systems is limited by the coherent state acquisition performed by the local oscillator. To get around this difficulty, it is needed to implement the circuit within the FHSS system that is able to rapidly generate a coherent carrier. The work presented in this paper proposes a realization of Costas loop based on a combination of Direct Digital Synthesis (DDS), (Temperature-Compensated) Voltage-Controlled Oscillator ((TC)VCXO), and Phase-Locked Loop (PLL), which in particular enables a short period (less than 100 μs) required for a local oscillator to reach the coherent state. The implemented model is thoroughly described with measurements results also provided.**

Index Terms—**Costas loop, DDS, PLL, carrier, FHSS.**

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I. Introduction

THE carrier signal synchronization is prerequisite for an application of a coherent demodulation method. In coherent communication systems, the technique of carrier synchronization is what drives the receiver structure. In general, there are two types of carrier synchronization techniques.

First type relies on a closed-loop phase which automatically tracks the carrier phase and use error feedback control to minimize the error in the received signal. Costas loop is most commonly used type of a closed-loop for carrier recovery [1]-[4]. This loop is not only adequate for a phase-based tracking of a suppressed carrier, but also for a demodulation of received signals. Therefore, the term 'Costas demodulator' is quite broad. Costas loop can be either analog or digital.

Second type relies on an open-loop phase with direct estimation of a phase error. Open-loop phase and frequency synchronization schemes are based on either the Maximum Apriori (MAP) or Maximum Likelihood (ML) parameter estimation principles. These are general feedforward techniques where the signal parameter is actively estimated and then treated as statistic for a detection algorithm [5].

The feed-forward compensation algorithm with direct phase offset estimation using in-phase and quadrature-phase demodulator outputs is presented in [6]. The feedback compensation algorithm with carrier synchronization that compensate a phase offset using the feedback loop, and signal conversion to baseband performed by the receiver, is described in [7]. Lately, turbo synchronization time and frequency based methods have emerged. Turbo synchronization using an iterative Expectation-Maximization (EM) algorithm used to estimate carrier phase, frequency offset or timing within a turbo receiver is proposed in [8]. More specifically, carrier phase estimation within a turbo receiver in BPSK (Binary Phase Shift Keying) and QPSK (Quadrature Phase Shift Keying) systems is described in [9]. Turbo decoders involve significant mathematical operations which restricts their use in FHSS systems. Previously mentioned techniques use either feedback-loop with very small noise bandwidth or feed-forward schemes which use training-sequences or symbol sequences in order to perform the time and frequency synchronization. These techniques might have relatively long acquisition time, and are not adequate for carrier synchronization in systems with short data packets.

Previous analysis demonstrates that fast carrier recovery has not been prioritized research activity. The fact that FHSS systems almost exclusively use incoherent demodulation methods proves our statement. Unlike the related work, this paper proposes a solution based on Costas loop, which enables fast carrier recovery. Proposed and implemented solution has the potential to be used for coherent demodulation in FHSS systems.

II. Proposed Model

Costas loops are being used in analog and digital communication systems for carrier synchronization. Moreover, Costas loop can be used for carrier recovery from double-sideband suppressed carrier signals. A circuit scheme of classical Costas loop used for coherent demodulation of BPSK

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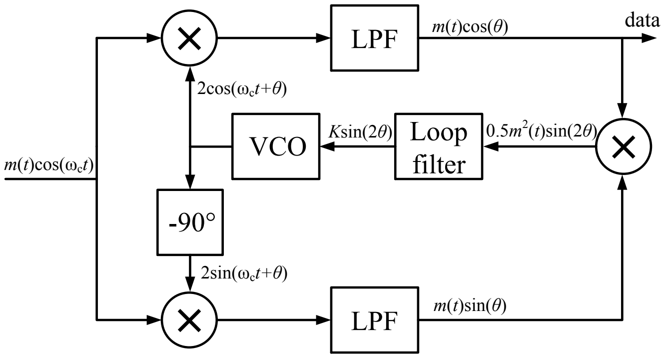

Fig. 1. A classical circuit scheme of Costas loop.

signals is shown in Fig 1.

The input signal is RF BPSK modulated signal $m(t)\cos(\omega_c t)$, which is a product of the transmitted data m(t)=±1 and the high frequency carrier $\cos(\omega_c t)$, where $\omega_c = 2\pi f_c$, and f_c denotes input signal carrier frequency. The sinusoidal voltage-controlled oscillator (VCO) signal is represented by $2\cos(\omega_c t+\theta)$, where θ is an implicit time function representing the portion of total signal phase not included in $\omega_c t$. On the upper branch the input signal is multiplied by the output signal of VCO, and signal $m(t)\cos(\theta)$ is obtain at the output of low-pass filter (LPF). On the lower branch the input signal is multiplied by the VCO signal, shifted by –90°, and then low-pass filtered obtaining the signal $m(t)\sin(\theta)$. Signal of form $0.5m^2(t)\sin(2\theta)$ is obtained after both branches being multiplied together. This signal is then filtered by the loop filter in order to provide control signal $K\sin(2\theta)$, which is used to adjust VCO frequency to the frequency of the input signal carrier. By reducing the phase error to zero, the VCO signal is synchronized with the carrier, and demodulated data are obtained on the upper branch. Thorough analysis of Costas loop with the noise influence on the loop performance can be found in technical literature.

The proposed Costas loop is based on direct digital frequency synthesis (DDS) and voltage-controlled crystal oscillator (VCXO), as shown in Fig. 2. The VCO and phase shifter in the classical model given in Fig. 1, is replaced by DDS and VCXO. The VCXO or temperature-compensated voltage-controlled crystal oscillator (TCVCXO) is used as a reference clock for DDS. The TCVCXO is more temperature stabile than VCXO resulting in a lower frequency mismatch between the input signal carrier and DDS output signal. Therefore, this configuration has a lower acquisition time. In addition, DDS allows faster frequency change when used as a local oscillator (LO). It can output two signals whose frequencies and phase difference can be adjusted with very high resolution (order of mHz and less than degree, respectively). Due to high frequency and phase resolution, in-phase and quadrature-phase signals can be provided by a single DDS chip.

The main advantage of this model of Costas loop is the ability to generate very fast and precisely both in-phase and quadrature-phase signals in complete DDS operating range.

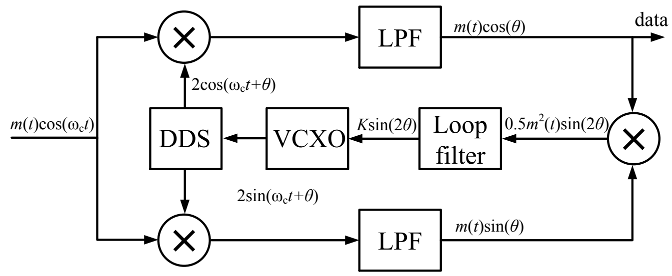

Fig. 2. A circuit model of Costas loop based on DDS and VCXO.

This allows the usage of Costas loop in reconfigurable radio and FHSS systems. In-lock state of the Costas loop is achieved when there is no frequency and phase mismatch between input signal and DDS output signals.

Considering fixed frequency scenario, the mean acquisition time T_{acq} consists of phase recovery time T_p and frequency recovery time $T_{\Delta f}$ [10]. For the second order PLL, it is given by

$$T_{acq} = T_p + T_{\Delta f} = \frac{4}{\omega_n} + \frac{4.2(\Delta f)^2}{B_L{}^3}. \quad (1)$$

where ω_n denotes PLL's natural frequency, B_L is PLL's bandwidth, and Δf is initial frequency mismatch. One can see that the frequency recovery time is proportional to the square of frequency mismatch. Phase and frequency recovery (locking) times as a function of frequency difference between the input signal carrier and local carrier are given in Fig 3.

Practical VCOs can have frequency mismatch of several kHz or MHz, which would have negative impact on frequency acquisition time. When there is no input signal, TCVCXO will oscillate at the frequency of crystal oscillator. Due to its relatively high temperature stability (0.28-2 ppm), DDS can be set very close to nominal frequency of the input signal carrier. This way, during the acquisition process, TCVCXO will reduce the frequency mismatch very fast, while phase recovery time would depend on natural frequency ω_n. For example, considering TCVCXO with frequency stability of ±1 ppm and

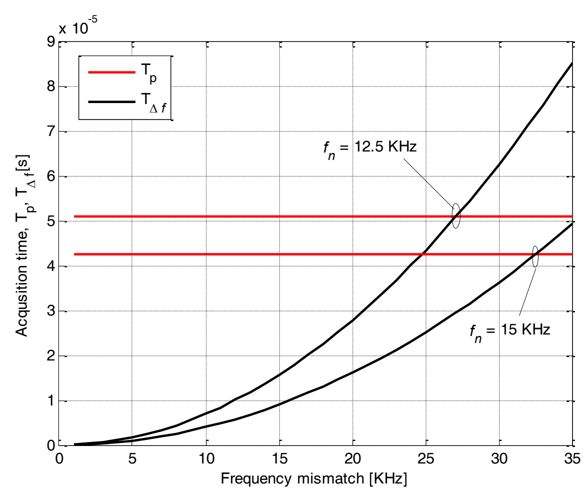

Fig. 3. Phase and frequency acquisition times.

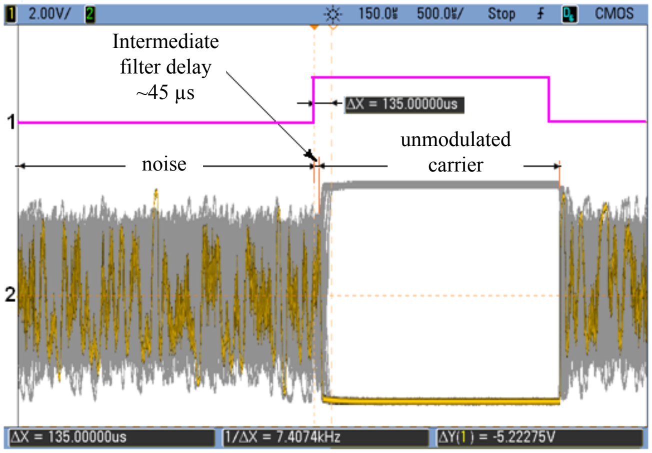

Fig. 4. Coherent state acquisition in Costas loop.

nominal frequency of 100 MHz, maximal frequency difference between the input signal carrier and local carrier is $\Delta f = 200$ Hz. For the second order PLL with natural frequency $f_n \approx 12.5$ KHz, damping factor $\xi \approx 0.7$, and $B_L = \omega_n/2(\xi+1/4\xi) \approx \pi f_n = 39.2$ KHz, time need to reduce frequency error can be assumed negligible, while mean phase acquisition time is 51 µs. Frequency recovery time gets higher with the increase of frequency difference, and becomes the same as phase recovery time for $\Delta f = 27$ KHz. With further increase of input signal carrier and local carrier frequency mismatch, the frequency recovery time becomes larger than phase recovery time.

The above analysis is referred to the fixed frequency scenario. In frequency agile systems, such as FH radios, where an agile local carrier is required, maximal frequency mismatch is equal to overall available bandwidth. In this case, if VCO is used as a local oscillator, frequency acquisition time would be very high. However, in the model with DDS and TCVCXO, the frequency acquisition time is negligible compared to the time needed for phase recovery. Using higher natural frequency, thus allowing additional noise, one can reduce the loop-locking time. However, more noise power is causing abrupt change of phase of local carrier during the transmission, which further causes change of polarity of demodulated signal. Therefore, PLL should have greater natural frequency during the acquisition and a lower natural frequency afterwards. However, a proper moment of switching from one value of natural frequency to another is not an easy task, especially at low signal-to-noise ratios, which may be the subject of a future research.

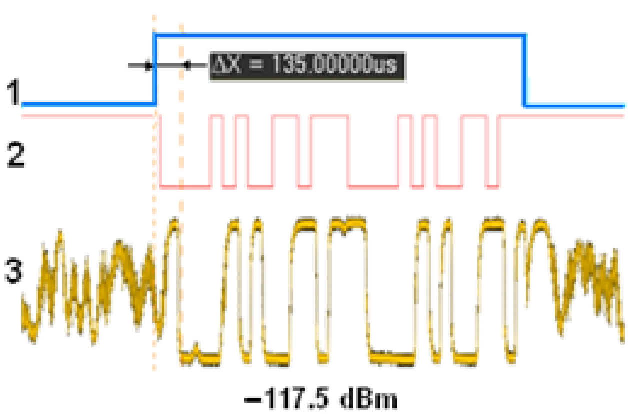

Fig. 5. The control signal (1), sequence (2) and demodulated signal (3).

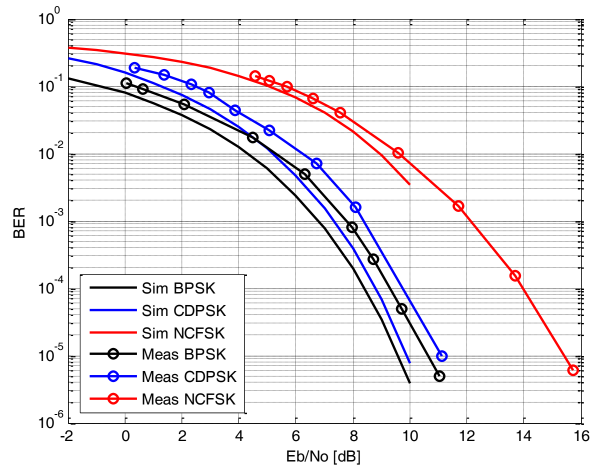

Fig. 6. BER as a function of E_b/N_0.

III. Measurements Results

Fig. 4 shows PLL coherent state acquisition time with natural frequency $f_n \approx 12.5$ KHz and damping factor $\xi \approx 0.7$. In order to measure the time period of interest, an input burst on-off keying (OOK) signal is used, as well as the VCXO. Signal 1 in Fig. 4 represents the modulating signal, whereas signal 2 represents in-phase component of demodulated signal in Costas loop. As notable from the figure, carrier demodulation is finalized within 135 µs. Reducing this value by the 45 µs delay of an intermediate frequency filter, one gets the coherent acquisition time of Costas loop. Given the aforementioned parameters and the frequency mismatch between the local and received signal of $\Delta f = 1$ KHz, the time needed to acquire coherent state (acquisition time) is less than 100 µs.

Fig. 5 shows demodulated signal when RF signal level is set to -117.5 dBm. The modulating signal is given in a form of the short pseudo random (PN) sequence, making the receiving RF signal in a form of a burst signal, which is quite typical for radars and FHSS systems. For proper demodulation of first receiving bits from the PN sequence, it is required that the phase loop is in its coherent state. This means that the transmitter should start emitting the carrier before information data (or sequence) is being sent.

Minimal carrier emitting time corresponds to loop-locking time (acquisition of coherent state), which is less than 100 µs, as stated before. It is demonstrated that the fast carrier generation at the transmitter is feasible [11], while keeping the phase noise and spurious signals at low level.

Theoretical and measured bit-error-rate (BER) as a function of signal-to-noise ratio (E_b/N_0) for BPSK, Coherent Differential PSK (CDPSK), and incoherent Frequency Shift Keying (FSK) is shown in Fig. 6. Measured BER for BPSK modulated signal is slightly worse relative to the theoretical

BER for BPSK modulated signal (≤ 1dB). Nonetheless, Fig. 6 illustrates that coherent demodulation of BPSK modulated signal significantly outperforms incoherent demodulation of FSK modulated signal. As we already stated, to reduce the acquisition time, it is required to broaden the loop bandwidth (larger ω_n). However, this leads to an increased power of the noise. The trade-off between the time of the coherent state acquisition and BER might be in usage of the coherent detection of the differential PSK (CDPSK) signal, whose theoretical and measurements results are presented in Fig. 6. Due to the difficulties observed in carrier phase tracking in FHSS communication system, incoherent FSK and Binary Frequency Modulation (BFM) are mainly deployed. Using BPSK modulation technique in these systems, however, requires extremely fast acquisition time at the beginning of each hop interval.

IV. Conclusion

In this paper a model of the Costas loop based on direct digital synthesis and phase-locked loop has been proposed and analyzed. Results of the measurement have confirmed a high performance of the model in terms of acquisition time and bit-error-rate at low signal-to-noise ratios. The proposed model has showed a very fast carrier recovery time (less than 100 μs), and when combined with CDPSK modulation, it allowed coherent demodulation in FH radios. CDPSK had up to 3-4 dB better performance by means BER relative to NCFSK. Finally, the proposed model of carrier synchronization can be applied in reconfigurable radio systems.

References

[1] R. E. Siferd and K. Xue, Costas Phase Locked Loop for BPSK Detection, Wright State University, 2008.

[2] B. Shamla and D. Gayathri, “Design and Implementation of Costas Loop for BPSK demodulator”, IEEE India Conference (INDICON), 2012.

[3] M. Roddewig, S.A. Zekavat and S. Nooshabadi, “Design of a Costas loop downconverter”, in 52. IEEE International Midwest Symposium on Circuits and Systems (MWSCAS’09), pp. 244-247, 2-5 Aug. 2009.

[4] Z. Yang, Y. Bai, Z. Zhao, “Design and Implementation of the Digital Costas Loop Based on Software Defined Radio”, First International Conference on Instrumentation Measurement, Computer, Communication and Control, 2011.

[5] S.P. Nicoloso, An Investigation of Carrier Recovery Techniques for PSK Modulated Signals in CDMA and Multipath Mobile Environments. Blacksburg, Virginia, June 1997.

[6] M. Nezami. Synchronization in Digital Wireless Radio Receivers. Florida Atlantic Univ., Doctoral dissertation, May 2001.

[7] Y. Liuand and C. Tao, “Feedback Compensation Algorithm for BPSK/QPSK Carrier Synchronization”, Radio Engineering, vol. 19, no. 1, pp.149-154, 2010.

[8] N. Noels, C. Herzet, A. Dejonghe, V. Lottici, H. Steendam, M. Moeneclaey, M. Luise, and L. Vandendorpe, “Turbo Synchronization: an EM Algorithm Interpretation,” in Proc. IEEE ICC , Vol. 4, pp. 2933-2937, May 2003.

[9] L. Zhang and A. G. Burr, “Iterative Carrier Phase Recovery Suited to Turbo-Coded Systems,” IEEE Trans. Wireless Comm., Vol. 3, pp. 2267-2276, Nov. 2004.

[10] V. Manassewitsch, Frequency Synthesizers Theory and Design, Third Edition, New York, N.Y., John Wiley and Sons, 1987

[11] S. Šajić, N. Maletić, M. Šunjevarić and B. Todorović, “Hybrid DDS-PLL Frequency Synthesizer with Reference Clock Modulation”, Frequenz, Vol. 67, No. 7–8, pp. 233–236, 2013