Telescopic Op-Amp Optimization for MDAC Circuit Design

Abdelghani Dendouga and Slimane Oussalah

***Abstract*—An 8-bit 40-MS/s low power Multiplying Digital-to-Analog Converter (MDAC) for a pipelined-to-Analog to Digital converter (ADC) is presented. The conventional dedicated operational amplifier (Op-Amp) is performed by using telescopic architecture that features low power and less-area. Further reduction of power and area is achieved by using multifunction 1.5bit/stage MDAC architecture. The design of the Op-Amp is performed by the elaboration of a program based on multi objective genetic algorithms to allow automated optimization. The proposed program is used to find the optimal transistors sizes (length and width) in order to obtain the best Op-Amp performances for the MDAC. In this study, six performances are considered, direct current gain, unity-gain bandwidth, phase margin, power consumption, area, slew rate, thermal noise, and signal to noise ratio. The Matlab optimization toolbox is used to implement the program. Simulations were performed by using Cadence Virtuoso Spectre circuit simulator in standard AMS 0.18µm CMOS technology. A good agreement is observed between the results obtained by the program optimization and simulation, after that the Op-Amp is introduced in the MDAC circuit to extract its performances.**

***Index Terms*—Analog circuit design; MDAC; MOGAs; operational amplifier; pipelined ADC.**

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I. Introduction

HIGH-speed, high-resolution and low-power design is becoming the chief research domain of Data converters. Analog-to-Digital Converter (ADC) and Digital-to-Analog Converter (DAC), play a fundamental role in interfacing the digital processing core with the outer real analog world. ADCs can be found in a wide range of applications, spanning from imaging to ultrasound and communication systems. In particular, pipelined ADC architecture [1-3] offers a good trade-off between conversion rate, resolution and power consumption.

Operational amplifiers (Op-Amps) are one of the most widely used building blocks for ADCs. To fulfill the given requirements, the designer must choose the suitable circuit architecture, although different tools which partially automated the topology synthesis appeared in the past [4-5]. Therefore, the use of multiple-objective optimization algorithms (MOGAs) is of a great importance to the automatic design of Op-Amp. Accuracy, ease of use, generality, robustness, and reasonable run-time are all necessary for a circuit synthesis solution to gain acceptance by using optimization methods [6-8]. This method uses a program based on multi-objective optimization using a genetic algorithm (GA) to calculate the optimal transistors dimensions (length and width) of transistors, of an Op-Amp which is used in the Multiplying Digital–to-Analog Converter (MDAC). The method which handles a wide variety of specifications and constraints, is extremely fast, and results in globally optimal designs.

The goal of this work is to design and optimize an MDAC circuit for a pipelined ADC in the sight of a front-end electronics of the semiconductor tracker (SCT) detector in ATLAS (A Toroidal LHC Apparatus) experiment [9]. This experiment will learn about the basic forces that have shaped the universe since the beginning of time.

This paper is organized as follows. The current section gives an introduction to the structure of this paper, the context of this work and the challenges for its completion. In section 2, the pipelined ADC structure is analyzed. Section 3 describes a MDAC circuit to be designed. The requirements and the optimization of the telescopic Op-Amp for the MDAC are described in section 4. Section 5 presents the MOGAs optimization methodology. Simulation results are presented in Section 6. Finally, some concluding remarks are given in the last section.

II. The Pipelined ADC

The pipeline ADC is composed with a non-overlapping clock generator, a sample-and-hold amplifier, N stages pipelined 1.5-bit/stage with 0.5-bit over range ADCs and DACs [10], a latch array, and a digital error correction circuit (Fig. 1). A non-overlapping clock generator will provide overall ADC non-overlapping clock phase. First, sample-and-hold amplifier will sample the input analog signal in the sample mode, and then hold this value in the output in the hold mode. The hold value will be transferred to digital by N-stage pipelined 1.5-bit/stage ADC (Fig. 2), and its code can be stored by the latch array. At last the digital error correction

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circuit corrects the error that is produced by each ADC stage offset, so the correct digital codes can be got in the output of the overall ADC.

III. THE MDAC

The MDAC is a single switched capacitor circuit that can be implemented the function of S/H operation, D/A conversion, subtraction, and amplification of the remainder. With the charge conservation concept, the output in hold phase is given by [2]:

$$V_{out} = \left(\frac{C_f - C_s}{C_f}\right) \cdot Vin - \left(\frac{C_s}{C_f}\right) \cdot V_{DAC} \quad (1)$$

where C_S is the sampling capacitor, C_F is the feedback capacitor, and V_{DAC} is the output voltage of the DAC circuit in the MDAC circuit. The MDAC circuit in the 1.5-bit/stage architecture is very simple as shown in Fig. 3.

The implementation of the MDAC stage is shown in Fig. 3 [2]. During the first phase, the input signal is sampled onto the sampling capacitors C_S and C_F. In the next phase, called amplifying phase, capacitor C_F is switched into feedback around the amplifier and C_S is connected to the voltage reference level, causing the charge redistribution that results in a signal amplification and subtraction by the voltage reference. Table I lists summary information about the 1.5-bit stage configuration.

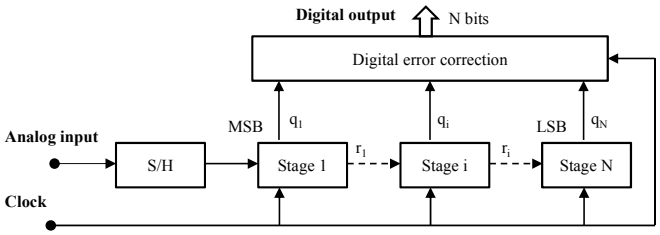


Fig. 1. Architecture of the pipelined ADC.

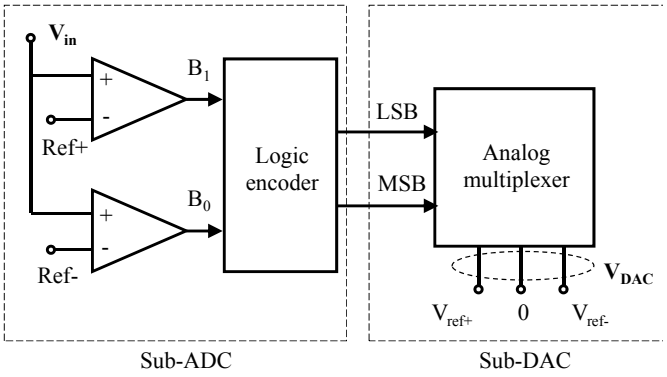


Fig. 2. Architecture of the 1.5 bit sub-ADC and DAC.

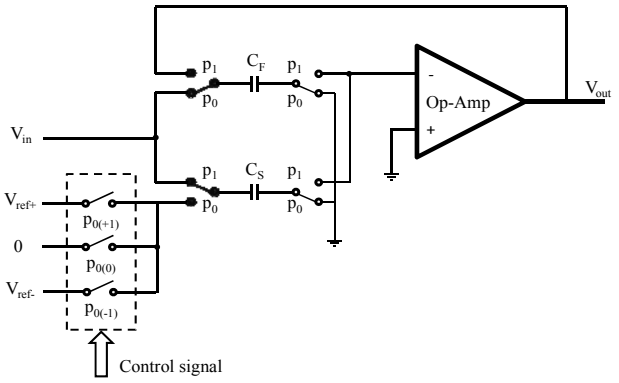


Fig. 3. MDAC circuit for a pipelined ADC.

TABLE I
SUMMARY INFORMATION FOR FIG. 2

V_{in}	Range	B1	B0	V_{DAC}	Analog residue
$V_{in}>Ref+$	High	1	0	V_{ref+}	$2V_{in}-V_{ref+}$
$Ref-<V_{in}<Ref+$	Middle	0	1	0	$2V_{in}$
$V_{in}<Ref-$	Low	0	0	V_{ref-}	$2V_{in}+V_{ref-}$

IV. AMPLIFIERS

Amplifiers in pipeline ADCs have a direct and major role in the operation of the individual pipeline stages by performing active sampling and residue amplification [6]. Consequently, the amplifier limitations have a direct impact on the overall ADC performance, which for high speed and very high resolutions may require the ADC to be digitally calibrated.

A. Op-Amp Requirements

The bandwidth and gain characteristics are crucial in the design of data converters. The Op-Amp is preferred to have 90° phase margin over full load conditions and process variations to avoid second order step response and its associated ringing. Decreasing the phase margin results in an increase of amplitude of ringing and this can increase the settling time. It can be proved that the DC open loop gain of an Op-Amp used in an ADC must satisfy the condition [11]:

$$A_0 \geq 2^{N+2} \quad (2)$$

where N is the number of bits of conversion.

In this work an 8 Bit data converter needs a minimum DC open loop gain of 54. The speed of an Op-Amp is decided by the Op-Amp used. The minimum unity gain frequency (f_u) for a given settling time ($t_s<1/f_{clk}$) required to settle the output to within +½ LSB of its final value can be evaluated as [11]:

$$f_u \geq 0.22(N+1) \cdot f_{clk} \quad (3)$$

i.e. for a 8 bit ADC at 40 MHz clock frequency needs an Op-Amp with a unity gain frequency of around 160 MHz.

Op-Amps are the key elements in analog-to-digital converter systems. For this reason, those circuit implementations that are specifically used to achieve the Op-Amp function in MDAC block. We have chosen the telescopic architecture to implement the Op-Amp because of its advantages. The telescopic amplifier is a single stage amplifier that exhibits one dominant pole, so it typically has higher frequency capability and consumes less power than other topologies, moreover its speed is higher than most other types of amplifiers [3].

B. Telescopic Op-Amp Architecture

The simplest version of a single stage Op-Amp is the telescopic architecture, shown in Fig. 4. The input differential pair injects the signal currents into common gate stages. Then, the circuit achieves the differential to single ended conversion with a cascode current mirror. We note that the transistors are placed one on the top of the other to create a sort of telescopic composition [4].

The most important of specification are the following:

– *Differential DC gain*

The differential DC gain is given by the expression:

$$A_V = gm_1 \cdot \frac{gm_6}{i_2^2\left(\lambda_n^2 + \lambda_p^2\right)} \tag{4}$$

– *Unity gain bandwidth*

The UGBW established by the dominant node is given by:

$$UGBW = \frac{gm_1}{C_L} \tag{5}$$

– *Slew rate*

For this Op-Amp, the condition to ensure a minimum slew rate is expressed as:

$$SR = \frac{I_{bias}}{C_L} \tag{6}$$

– *Phase margin*

The phase margin is given by:

$$PM = 180 - \tan^{-1}\left(\frac{GBW}{p_1}\right) - \tan^{-1}\left(\frac{GBW}{p_2}\right) - \tan^{-1}\left(\frac{GBW}{z}\right) \tag{7}$$

– *Power consumption*

The power consumption of this operational amplifier can be calculated as follows:

$$P = \left(V_{DD} - V_{SS}\right) \cdot I_{bias} \tag{9}$$

– *Area*

The area occupied by the Op-Amp circuit is given by:

$$Area = \sum_{i=1}^{k} W_i \cdot L_i \tag{8}$$

In practice, the area must take into account all the connections respecting the design rule check (DRC) of the technology that can take a non-negligible space area. So, this approximation must be improved.

The Op-Amp, forming the core of a switched capacitor (SC) multiplying D/A converter, is the most critical block of a pipeline stage [6]. The resolution and speed of the whole ADC is usually determined by the Op-Amps of the MDACs. Usually, the amplifiers open loop DC-gain limits the settling accuracy of the amplifier output, while the bandwidth and slew rate of the amplifier determine the maximal clock frequency.

To maximize the signal-to-noise ratio, the Op-Amp should also utilize a large signal swing at the output. The amplifier specifications relative to the resolution and sample rate i.e, the DC-gain of the amplifier in a MDAC is determined by the resolution, and the slew rate and GBW specifications can be derived from the sampling speed of the A/D converter. The sampling speed of a pipeline A/D converter is in turn dictated by the settling time of the amplifier in the MDAC. The settling time is determined first by the slew rate (SR) and finally by the GBW of the amplifier.

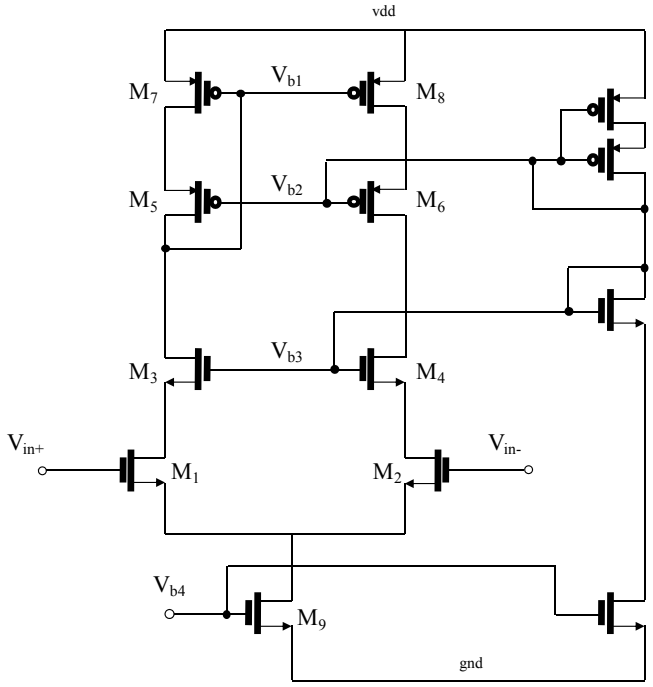


Fig. 4. Telescopic CMOS Op-Amp architecture.

V. MULTI-OBJECTIVE OPTIMIZATION

A. Genetic Algorithms

Optimal design of analog circuits is to find a variable set $x=\{x_1, x_2,\ldots,x_n\}$ that optimizes a performance functions, such as maximum operating frequency, gain, SNR, offset, etc.

Knowing that this variable meets imposed specifications and/or inherent constraints, for example, technology limits, saturation conditions of transistors, impedance matching, etc. Vector x may encompass biases, lengths (L) and widths (W) of MOSFET gate transistors, component values, etc. [5]. In the optimization stage the parameter space is explored and the design improved with respect to the objective functions [12,13]. The optimization, which is called multi-objective optimization, is based on an evolutionary algorithm known as weight-based GA [6]. Genetic algorithms are a particular class of evolutionary algorithms, that use biology inspired techniques such as selection, mutation, crossover and inheritance [2].

A weighted approach has been used to optimize Op-Amps. It uses adaptive weights along the optimization process to determine the overall fitness of an individual [10:].

$$F = \sum_{i=1}^{n} \omega_i \cdot f_i \tag{10}$$

where ω_i is the relative preference or weight associated with the objective function.

B. *Optimization Methodology*

The heart of the whole algorithm is the optimization engine; our optimization algorithm is developed in MATLAB and implemented in the MOGA optimization tool MATLAB. GA is responsible for the exploration of the solution space in the search for optimal solutions. In general, the best individuals in a population tend to reproduce.

At the beginning we generate the individual randomly n times (n represents the population size). The individual is made up of binary code string encoding a particular sized Op-Amp fitness of every individual can be got, and then the GA can be used to choose the better individuals as the parents of the next generation. After crossing and mutating, the new generation is produced. Performing the above works iteratively the goal will be achieved in the end (Fig. 6) [5].

In the program elaborated with MATLAB toolbox, every individual is presented by a binary code string. Fig. 3 shows that telescopic Op-Amp contains 9 CMOS transistors and biasing current (I_{bias}). As a total there are 11 parameters to be adjusted and each gene of the chromosome stands for one parameter. Thus, the parameter vector is compressed to [9]: [W_1, L_1, W_3, L_3, W_5, L_5, W_7, L_7, W_9, L_9, I_{bias}]. The size of the transistors M_2, M_4, M_6, and M_8 are equal to M_1, M_3, M_5, and M_7, respectively.

The goal of multi-objective optimization is the finding a vector x of decision variables satisfying constraints to give acceptable values to all objective functions fi(x). In this MOGA, six performances are considered: DC gain, unity-gain band width, phase margin, power, circuit area, and slew rate. The basic steps of GAs procedure is shown in Fig. 4.

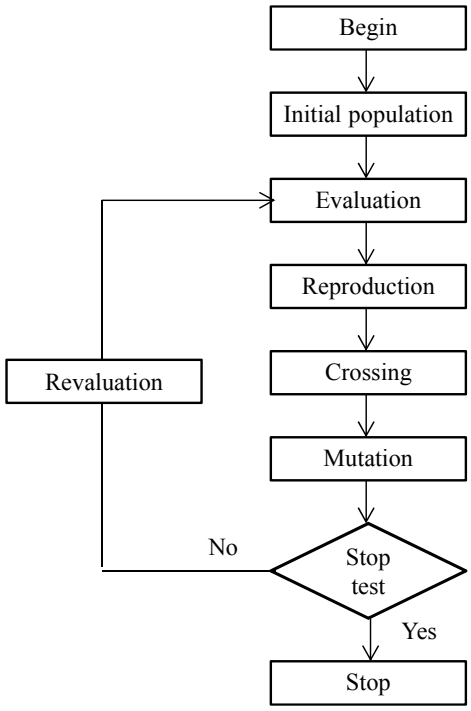


Fig. 5. Basic procedure of genetic algorithms.

VI. Results and Discussion

In this work, six performances are considered: bandwidth of unity-gain, DC gain, phase margin, power consumption, circuit area, slew rate, thermal noise and signal to noise ratio. Variables obtained from GAs (Table II) are used to simulate the two-stage Op-Amp circuit by using Cadence Virtuoso Spectre in AMS 0.18µm CMOS technology. The simulated DC gain and a phase margin of a telescopic Op-Amp are demonstrated in Fig. 6. The DC gain exhibits a high gain of 62.8 dB and a phase margin of 57.42° with the unity gain bandwidth of 285.8 MHz. Power consumption is evaluated at 0.051 mW.

By using variables obtained from GA (Table II), the telescopic Op-Amp circuit is simulated by using Cadence Virtuoso Spectre in AMS 0.18µm CMOS process. The results obtained by simulation shown in Fig. 7 and Table III confirm the efficiency of GA in determining the device sizes in analog circuits. Our results are compared to the results given in [16].

Consequently the performance of the telescopic Op-Amp optimized by the proposed method represents a good method to optimize an analog circuit.

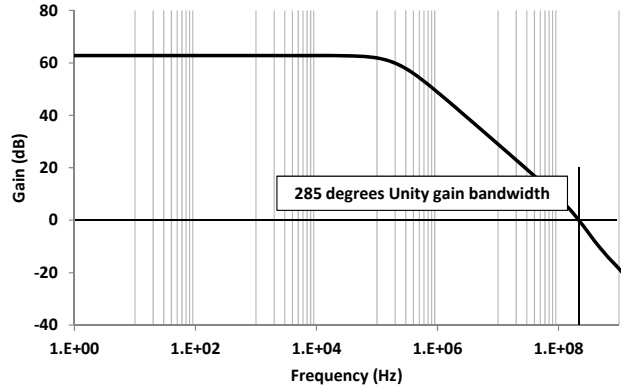
Wafer production will always show some variation of technological parameters (process parameters and mismatch parameters). The Monte Carlo process simulation is the adequate tool to give an early estimation how it will affect the circuits' function [14,15].

TABLE II
OPTIMAL TRANSISTORS DIMENSIONS

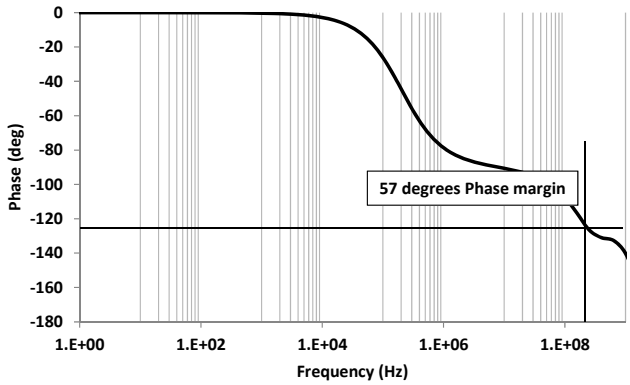
Variable	Min	Max	Chosen iteration	In circuit
W1=W2	15µm	35µm	25.4 µm	25µm
L1=L2	0.18µm	1µm	274 nm	0.28µnm
W3=W4	15µm	35µm	25.5 µm	25µm
L3=L4	0.18µm	1µm	345 nm	0.35µm
W5=W6	100µm	300µm	249 µm	250µm
L5=L6	0.18µm	1µm	294 nm	0.3µm
W7=W8	20µm	50µm	30.7 µm	30.7µm
L7=L8	0.18µm	1µm	326nm	0.33µm
W9	100µm	200µm	124 µm	125µm
L9	0.18µm	1µm	269 nm	0.27µm
I_{bias}	5µA	200µA	158µA	160µA

TABLE III
PERFORMANCE OF THE DESIGN OBTAINED BY MATLAB OPTIMIZATION PROGRAM COMPARED TO SPECTRE SIMULATION RESULTS

Performance Names	Specification Values	MOGA program	Spectre Simulation	[16]
Supply Voltage (V)	1.8	1.8	1.8	3.3
DC Gain dB)	≥ 54	62	62.81	90
Unity GBW (MHz)	≥ 160	280	285.8	90
Phase Margin (deg)	≥ 50	60	57.42	78
Slew Rate (V/µs)	Max	2.25	2.19	0.125
Area (µm²)	Min	559	580-	-
Power (mW)	Min	0.047	0.051	-
Technology	AMS 0.18 µm	-	AMS 0.18 µm	0.18 µm



(a)



(b)

Fig. 6. Gain (a) and phase (b) diagrams of the telescopic CMOS Op-Amp.

Fig. 7 shows Monte Carlo analysis of the optimized telescopic Op-Amp. The Op-Amp was found to have a DC-gain variation of-0.565-mV over 200-runs, meaning a 3σ DC-gain of 1.69-mV, which keeps the gain upper than 54, and an unit gain bandwidth variation of 6.07 MHz, meaning a 3σ unit gain bandwidth of 18.21-MHz, which keeps the unit gain bandwidth upper than 160 and a phase margin variation of 0.52-deg, meaning a 3σ phase margin of 1.57-deg, which keeps the telescopic Op-Amp stable.

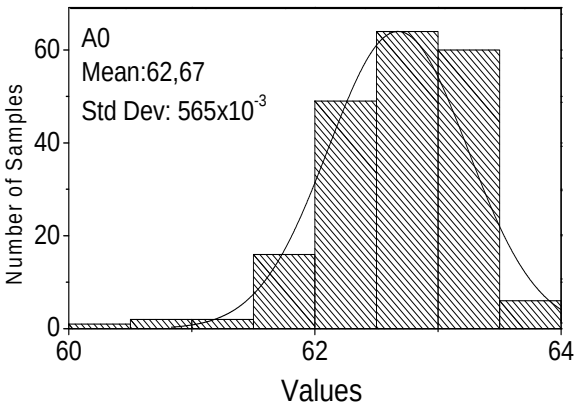
To check effectively the design, it is important to simulate if it works properly inside its real environment. Fig. 8 shows a testbench which realizes the complete MDAC as it will be printed on the silicon; the input of the system is fed by a ramp.

The main function of the sub-DAC is to output an analog voltage based on the comparators decisions. The residue plot shown in Fig. 9 represents the transfer function which is created by the switched capacitor circuit (MDAC). Fig. 10 represents the binary response of the 1.5 bit stage in the different three level of the reference signal.

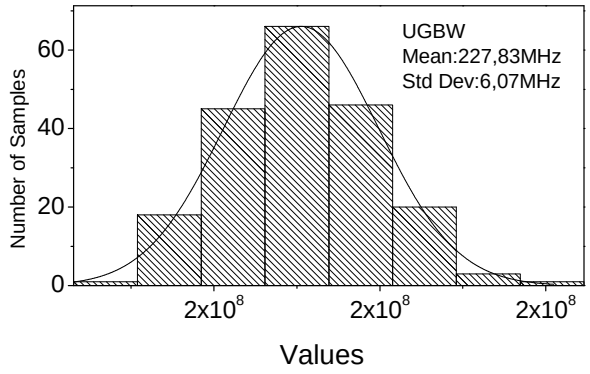
The transfer function of an ideal ADC can be represented by a best fit line as shown in Fig. 11, typically either an endpoint fit or a least squares fit.

An ADC that exhibits integral non-linearity (INL) will have a transfer function that is not a perfect line. The maximum difference between the actual and the ideal transfer characteristic is the INL. The telescopic Op-Amp is placed in the test bench illustrated in Fig. 7 to be simulated and its INL is calculated. This concept is illustrated in Fig. 11. We note

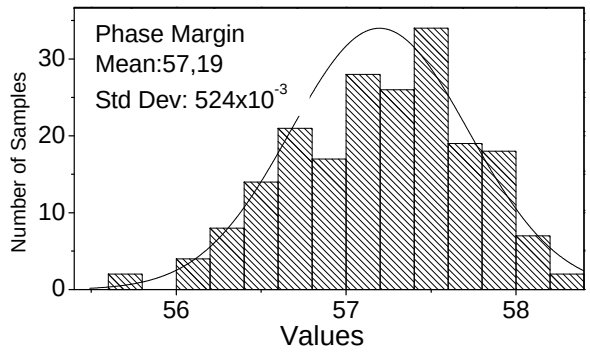
that telescopic architecture generates an INL error less than 3.5 LSB.



(a)



(b)



(c)

Fig. 7. Monte Carlo Simulation of (a) DC gain, (b) Unity Gain Bandwidth and (c) Phase Margin of the Telescopic Op-Amp.

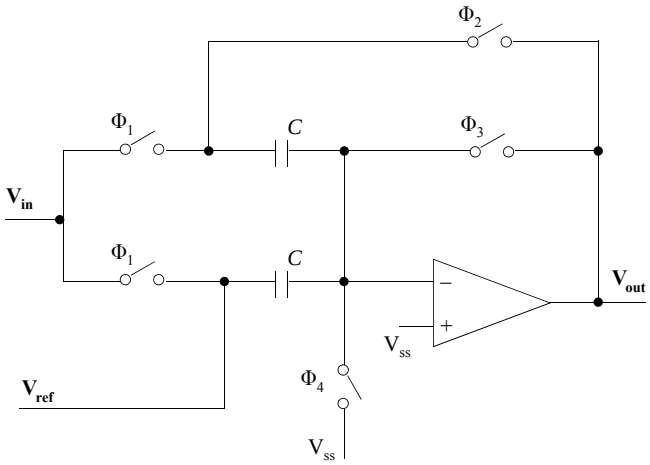


Fig. 8. The MDAC test bench.

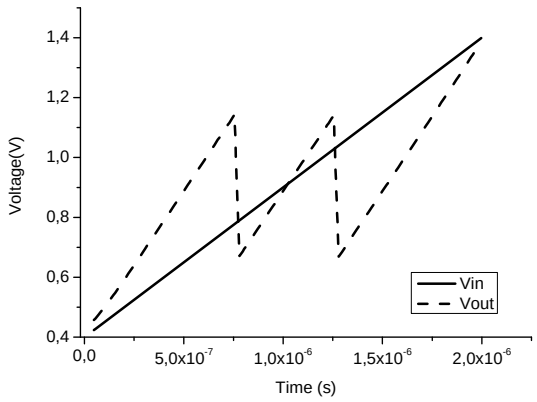


Fig. 9. The transfer function of the MDAC.

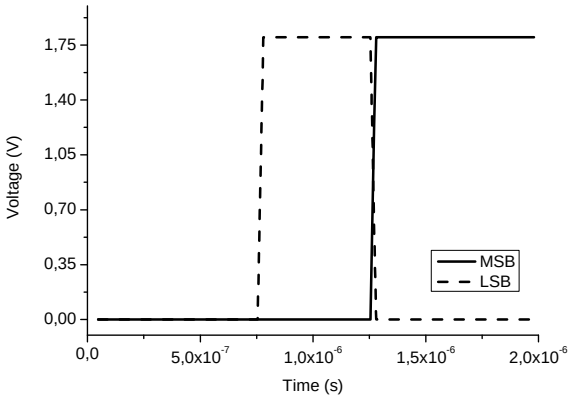


Fig. 10. Binary response of the MDAC for a ramp signal input.

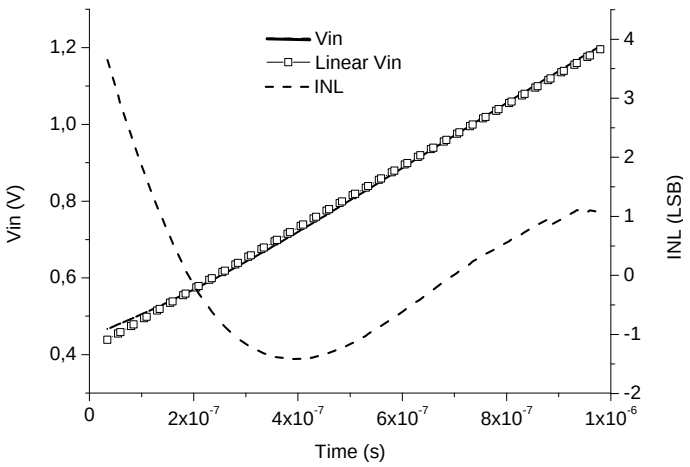


Fig. 11. Transfer Function of the MDAC and its Best Fitted Line and the INL of the MDAC Using Optimized Telescopic.

VII. CONCLUSION

This work has demonstrated the utility of an evolutionary algorithm for automating electronic design using algorithms called multi-objective genetic algorithms, which have the ability to deal with a problem of multi-objective optimization with two or more goals and taking account also the constraints. A program based on MOGAs has been developed to optimize the performances of a telescopic operational amplifier by determining its CMOS transistors sizes in order to design an optimized 8-bit 40-MS/s low power Multiplying Digital–to–Analog Converter (MDAC) for a pipelined ADC. The optimization procedure was implemented using MATLAB optimization toolbox, and the circuit simulation results were obtained from Spectre. The Op-Amp was designed in AMS 0.18µm CMOS technology.

Monte Carlo analysis of the optimized telescopic Op-Amp shows that DC-gain, unit gain bandwidth, and phase margin prove the effectiveness of the approach in the MDAC design where the design space is too complicated to be done with the classical methods within a short time. It can be concluded that the proposed MOGAs-based approach is efficient and gives promising results for circuits design and optimization problems.

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