A Novel Purely Active Electronically Controllable Configuration for Simulating Resistance in Floating Form

Mayank Srivastava and Dinesh Prasad

***Abstract*—This paper proposes a new purely active floating resistance simulation circuit employing two voltage differencing trans-conductance amplifiers (VDTAs). The proposed configuration enjoys following advantageous features; (i) purely active realization (ii) electronically tunable resistance (iii) no requirement of any active/passive component matching constraint (iv) good non-ideal behavior and (v) low sensitivity values. The Influence of VDTA terminal parasitics on high frequency behavior of proposed circuit is also investigated. The workability of proposed resistor simulator has been verified by an application example of voltage mode low-pass filter. To validate the theoretical analysis, SPICE simulations with TSMC 0.18µm CMOS process parameters have been performed.**

***Index Terms*— Active simulation, Electronic control, Floating resistance, VDTA**

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I. INTRODUCTION

ACTIVE simulation of floating passive elements (resistors/capacitors/inductors) is a fascinating research area for analog circuit designers and researchers. Several floating passive component simulators employing different active building blocks (ABBs) have been proposed in [1]-[18] and reference cited therein. The floating resistor is an integral part of many analog circuits but from the viewpoint of monolithic integration it is not advisable to use a resistor in floating form as a floating resistor need more chip area than a grounded resistor as well as it is very difficult to design such a resistor with exact resistance value. Moreover, the resistance of such resistor is fixed and cannot be changed as per requirement. So, the active simulation of floating resistors has become a popular research area in which a floating resistor is realized either by using active element(s) along with external resistor(s) or by using active element(s) alone. Many synthetic floating resistor configurations using different active elements such as operational amplifier (OP-AMP) [6], operational trans-conductance amplifier (OTA) [7], modified current feedback operational amplifier (MCFOA) [8], second generation current conveyor (CCII) [9]- [11], [14] differential difference current conveyor (DDCC) [12], current controlled second generation current conveyors (CCCII) [13], current backward trans-conductance amplifier (CBTA) [15]-[16], current follower trans-conductance amplifiers (CFTA) [17] and differential voltage second generation current conveyor (DVCCII) [18] have been reported in literature but unfortunately all of these proposed configurations suffer one or more of following disadvantages:

- Use of excessive number of active elements (more than two) [6], [9], [11], [13].
- Use of external resistor(s) [6]-[11], [14]-[16], [18].
- Non-availability of electronic control [6], [8], [9]-[11], [18].
- Need for active/passive component matching constraint(s) [16]-[17].
- Degraded non ideal performance [18].

Therefore, the aim of this paper is to propose a new purely active synthetic floating resistor configuration employing VDTA. The proposed realization employs only two VDTAs and exhibit following advantageous features; (i) no requirement of any external resistor (ii) electronically tunable resistance (iii) no requirement of any matching constraint (iv) good non- ideal behavior and (v) low active and passive sensitivities.

II. PROPOSED CONFIGURATION

The voltage differencing trans-conductance amplifier (VDTA) is one of the active elements which have been introduced in [19]. It provides currents and voltages at different terminals with electronically controllable trans-conductance gains. Therefore, VDTA block is very suitable for synthesis and design of active circuits with electronic control feature. Fig.1 shows the symbolic representation of VDTA, where P and N are input ports, z is auxiliary port and X+ and X- are output ports. All the ports of VDTA exhibit high impedance levels. The CMOS implementation of VDTA [20] has been shown in Fig. 2.

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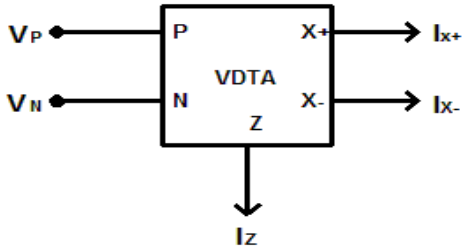

Fig. 1. VDTA symbolic representation

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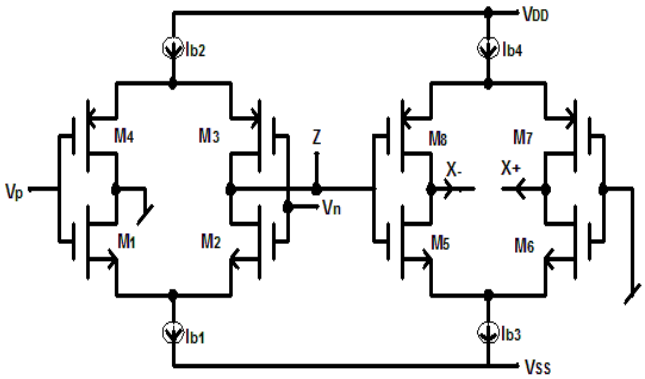

Fig. 2. CMOS implementation of VDTA [20]

The port relations of ideal VDTA shown in Fig.1 can be characterized by following hybrid matrix;

$$\begin{bmatrix} I_Z \\ I_{X^+} \\ I_{X^-} \end{bmatrix} = \begin{bmatrix} g_{m_1} & -g_{m_1} & 0 \\ 0 & 0 & g_{m_2} \\ 0 & 0 & -g_{m_2} \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \end{bmatrix}. \quad (1)$$

The trans-conductance gains g_{m1} and g_{m2} of CMOS VDTA shown in Fig. 2 are given as

$$g_{m_1} = \frac{g_3 + g_4}{2} \quad (2)$$

$$g_{m_2} = \frac{g_5 + g_8}{2} = \frac{g_6 + g_7}{2} \quad (3)$$

Where, g_n is the trans-conductance of n^{th} MOS transistor given as

$$g_n = \sqrt{I_{B_n} \mu_n C_{OX} \left(\frac{W}{L}\right)_n} \quad (4)$$

Where, μ_n is carrier mobility, C_{OX} is capacitance of gate-oxide layer per unit area, W is MOS transistor's effective channel width, L is effective channel length and I_{Bn} is bias current of n^{th} transistor.

VDTA find several applications in designing of analog filters [21]-[23], oscillators [24] and inductor simulators [25] but there is no application in simulation of floating resister has been reported so far. So, this paper is an effort to fill this void.

The proposed purely active floating resister simulator is shown in Fig. 3.

The Routine circuit analysis of configuration shown in Fig. 3 yields short circuit admittance matrix as;

$$\begin{bmatrix} I_{in} \\ I_{out} \end{bmatrix} = \frac{g_{m_1} g_{m_2}}{g_{m_3}} \begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix} \begin{bmatrix} V_{in} \\ V_{out} \end{bmatrix} \quad (5)$$

Which simulate a floating resistor with resistance value;

$$R_{eq} = \frac{g_{m_3}}{g_{m_1} g_{m_2}} \quad (6)$$

Where (g_{m1}, g_{m2}) and (g_{m3}, g_{m4}) are the trans-conductance gains of VDTA-1and VDTA-2 respectively.

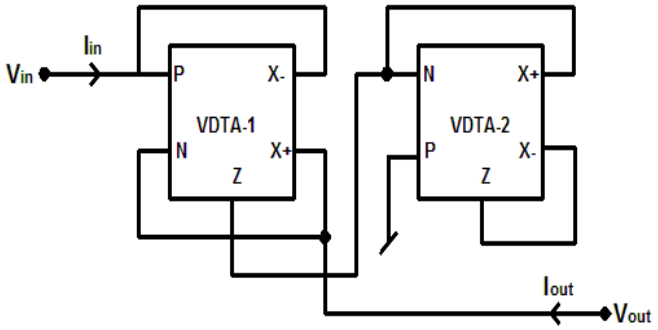

Fig. 3. Proposed purely active floating resistor simulator

One can observe from (6) that the resistance of proposed synthetic resistor can be controlled electronically by varying trans-conductance gains g_{m1}, g_{m2}, g_{m3}, and g_{m4}. It is important to note that the presented circuit can also simulate negative floating resistor (-R) by appropriate interchanging of p and n and/or x+ and x- ports of VDTAs. Such negative resistor simulator can be used for parasitic cancellation purpose.

III. Non-ideal Analysis

In the non-ideal ideal case, the VDTA can be characterized by the following equations

$$I_Z = \beta_Z g_{m_1} (V_P - V_N) \quad (7)$$

$$I_{X+} = \beta_{x+} g_{m_2} V_Z \quad (8)$$

$$I_{X-} = -\beta_{x-} g_{m_2} V_Z \quad (9)$$

where β_Z, β_{X+} and β_{X-} are non ideal trans-conductance gain errors.

To check the behaviour of presented configuration under non ideal conditions, it is revisited considering the non ideal model of VDTA described by (7)-(9). The short Circuit admittance matrixes and floating resistances values of proposed simulator under the influence of VDTAs non

idealities can be re-expressed as

$$\begin{bmatrix} I_{in} \\ I_{out} \end{bmatrix} = \frac{g_{m_1} g_{m_2} \beta_{x_1-} \beta_{x_2-} \beta_{z_1}}{g_{m_3} \beta_{x_2+} \beta_{z_2}} \begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix} \begin{bmatrix} V_{in} \\ V_{out} \end{bmatrix} \tag{10}$$

and

$$R_{eq} = \frac{g_{m_3} \beta_{x_2+} \beta_{z_2}}{g_{m_1} g_{m_2} \beta_{x_1-} \beta_{x_2-} \beta_{z_1}} \tag{11}$$

where (β_{Z1}, β_{X1+}, β_{X1-}) and (β_{Z2}, β_{X2+}, β_{X2-}) are the trans-conductance gain errors of VDTA-1 and VDTA-2 respectively.

It is clear from (11) that even under the non ideal conditions the proposed configuration simulates the lossless floating resistor.

The sensitivity figures of resistance of simulated floating resistor with respect to trans-conductance gains/ gain errors are found as;

$$\begin{aligned} &S_{g_{m1}}^{R_{eq}} = S_{g_{m2}}^{R_{eq}} = -1, S_{g_{m3}}^{R_{eq}} = 1, S_{g_{m4}}^{R_{eq}} = S_{\beta_{x1+}}^{R_{eq}} = 0, \\ &S_{\beta_{x2+}}^{R_{eq}} = S_{\beta_{z2}}^{R_{eq}} = 1, S_{\beta_{x1-}}^{R_{eq}} = S_{\beta_{x2-}}^{R_{eq}} = S_{\beta_{z1}}^{R_{eq}} = -1 \end{aligned} \tag{12}$$

So, all the sensitivity values are low and not more than unity in magnitude.

IV. Effects of Parasitic Impedances

At high frequency, the terminal parasitic of VDTA comes into the picture and effect the performance of a VDTA based circuit. A conventional VDTA along with its port parasitics has been shown in Fig. 4.

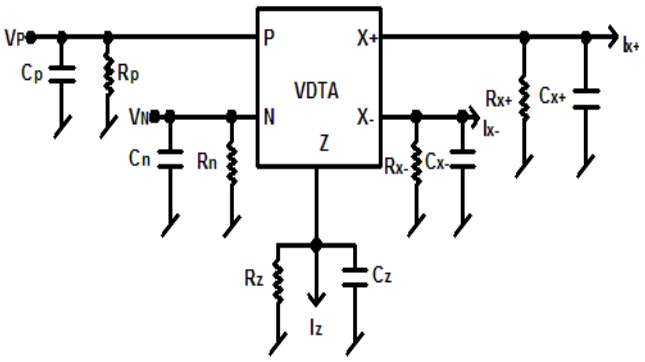

Fig. 4. Conventional VDTA with port parasitics

To study the effects of terminal parasitic of VDTAs on proposed resistance simulator configuration, this configuration was examined including port parasitics of VDTA. Fig. 5 shows the proposed resistance simulator with port parasitic of VDTA-1 and VDTA-2.

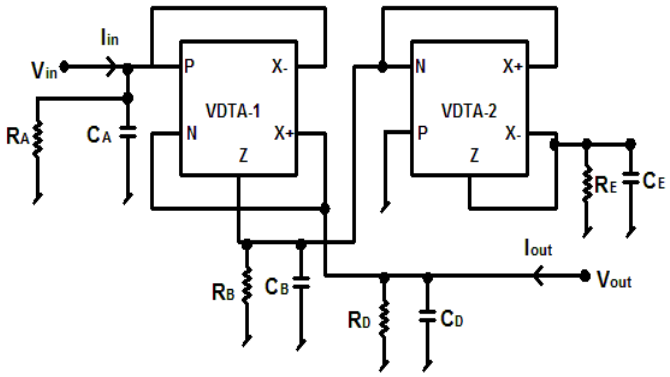

Fig. 5. Proposed configuration including the parasitics of VDTAs

$$R_A = \frac{1}{\frac{1}{R_{p_1}} + \frac{1}{R_{X_1-}}} \tag{13}$$

$$R_B = \frac{1}{\frac{1}{R_{z_1}} + \frac{1}{R_{n_2}} + \frac{1}{R_{x_2+}}} \tag{14}$$

$$R_D = \frac{1}{\frac{1}{R_{n_1}} + \frac{1}{R_{x_1+}}} \tag{15}$$

$$R_E = \frac{1}{\frac{1}{R_{z_2}} + \frac{1}{R_{x_2-}}} \tag{16}$$

$$C_A = C_{p_1} + C_{x_1-} \tag{17}$$

$$C_B = C_{z_1} + C_{n_2} + C_{x2+} \tag{18}$$

$$C_D = C_{n_1} + C_{x_1+} \tag{19}$$

$$C_E = C_{z_2} + C_{x_2-} \tag{20}$$

As the proposed configuration does not has any external passive component, so effects of port parasitic impedances cannot be alleviated and these parasitics will limit the high frequency behaviour of proposed configuration. So, the maximum usable frequency under the influence of parasitics can be found as:

$$\omega_{0_{max}} \langle\langle \min\left\{ \begin{array}{l} \dfrac{(\frac{1}{R_{p_1}}+\frac{1}{R_{x_1-}})}{(C_{p_1}+C_{x_1-})}, \dfrac{(\frac{1}{R_{n_1}}+\frac{1}{R_{x_1+}})}{(C_{n_1}+C_{x_1+})}, \\ \dfrac{(\frac{1}{R_{n_2}}+\frac{1}{R_{x_2+}}+\frac{1}{R_{z_1}})}{(C_{n_2}+C_{x_2+}+C_{z_1})}, \dfrac{(\frac{1}{R_{z_2}}+\frac{1}{R_{x_2-}})}{(C_{z_2}+C_{x_2-})} \end{array} \right\} \quad (21)$$

V. Application Example

The workability of proposed circuit is also verified by low-pass filter design example. The passive RC low-pass filter employing a floating resistor and a grounded capacitor has been shown in Fig. 6 and active realization of this low-pass filter using proposed resistor simulator is shown in Fig. 7.

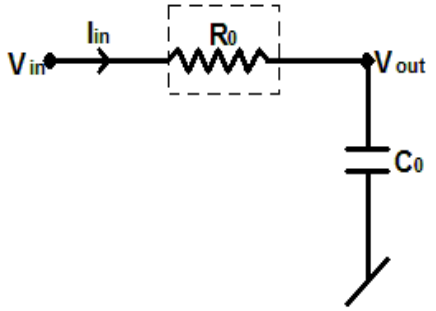

Fig. 6. Passive realization of voltage-mode low-pass filter

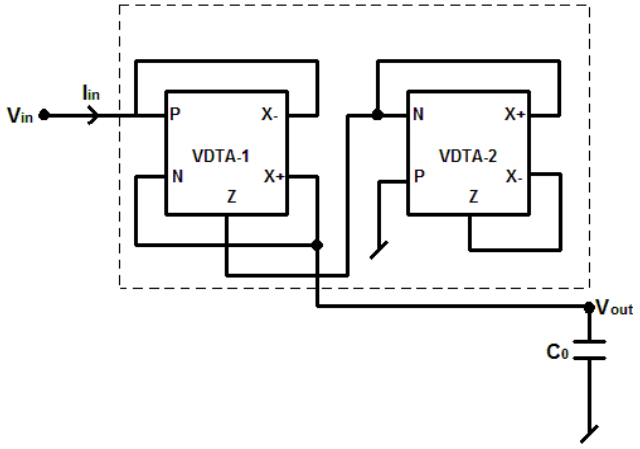

Fig. 7. Active realization of voltage-mode low-pass filter shown in Fig 6 employing proposed floating resistance simulator

The voltage mode transfer function obtained from Fig. 7 is given by equation (22), which is low-pass transfer function.

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{1+\dfrac{sC_0 g_{m_3}}{g_{m_1} g_{m_2}}} \quad (22)$$

VI. Simulation Results

The circuit illustrated in Fig.3 is tested by SPICE simulations with TSMC 0.18 µm process parameter model. The simulations were performed employing CMOS VDTA (shown in Fig. 2) with supply voltages ±0.9 VDC and bias currents $I_{b1}= I_{b2} = I_{b3} = I_{b4} = I_{b5} = I_{b6} = I_{b7} = I_{b8} = I_b = 150$ µA, where I_{b1}, I_{b2}, I_{b3} and I_{b4} are the bias currents of VDTA1 and I_{b5}, I_{b6}, I_{b7} and I_{b8} are the bias currents of VDTA2. The magnitude and phase response of impedance of proposed simulator have been shown in Fig. 8 and Fig. 9 respectively. It is seen from Fig. 8 that simulated magnitude response is approximately same as ideal magnitude response up to 292 MHz frequency (simulated resistance value is found 1.562 kΩ while ideal value is 1.571 kΩ upto 292 MHz). The phase responses as shown in Fig. 9 clearly indicate that simulated phase response matches the ideal phase response up to 34 MHz frequency. The deviation of simulated responses from ideal responses at high frequencies is due to presence of VDTA parasitic impedances. To demonstrate the electronic control of proposed configuration, simulations have been performed for different set of bias currents. Fig. 10 illustrated the magnitude responses for I_b = 130 µA, 110 µA and 90 µA. The simulated floating resistance values for I_b = 130µA, 110 µA and 90 µA were found 1.667, 1.816 kΩ and 2.002 kΩ respectively, while the ideal values were 1.689 kΩ, 1.836 kΩ and 2.029 kΩ. Hence, the deviation between simulated values and ideal values is not more than 1.5% in limited frequency region. The low-pass filter shown in figure 7 is also simulated using CMOS VDTA with supply voltage of ±0.9 VDC. The value of capacitor C_0 is chosen as 0.1nF. The SPICE simulated frequency responses of this filters is shown in Fig. 11.

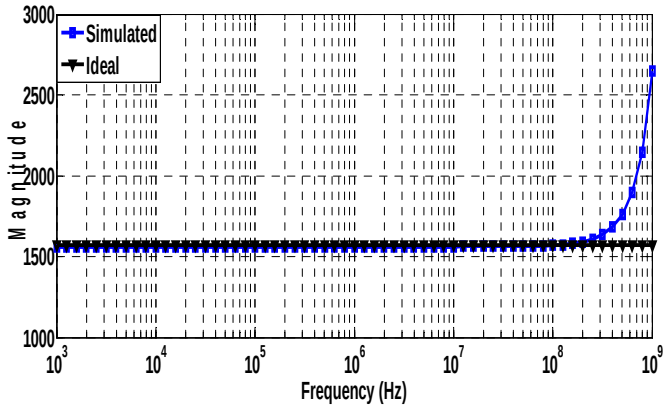

Fig. 8. Magnitude response of input impedance of proposed simulator

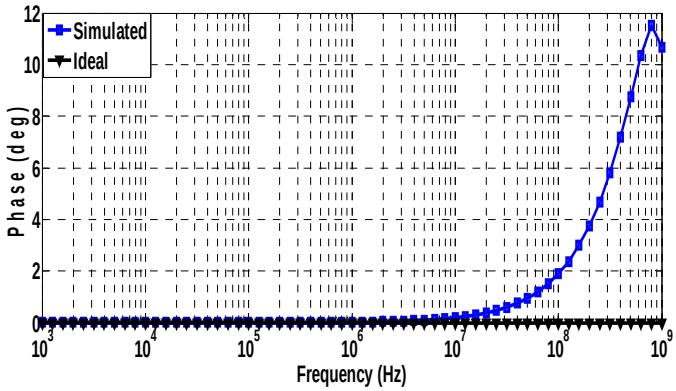

Fig. 9. Phase response of input impedance of proposed simulator

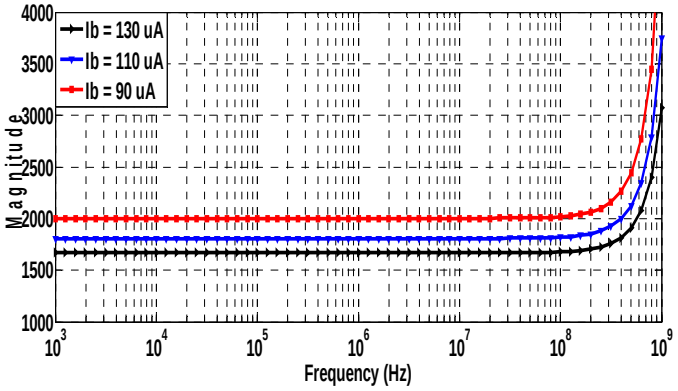

Fig. 10. Magnitude responses for different bias currents

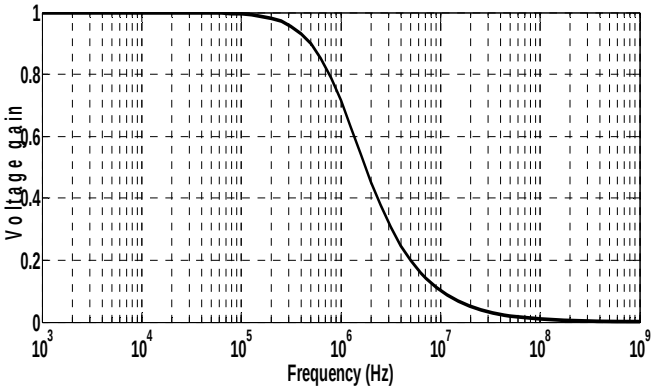

Fig. 11. Frequency response of low-pass filter shown in Fig. 7

VII. Conclusion

A new purely active floating resistor simulator employing two VDTAs has been presented. To the best knowledge of authors there is no purely active floating resistor simulator employing VDTA(s) has been available in literature. The proposed configuration enjoys electronically tunable resistance, low sensitivity values, no requirement of any component matching constraint and excellent non-ideal behavior. The effects of port parasitics of VDTAs also have been investigated in proposed circuit to define high frequency limitation. The application of proposed resistor simulator in designing of a low pass filter has been proposed and verified. The mathematical analysis has been verified by SPICE simulations with TSMC 0.18µm CMOS process parameters.

References

[1] S. Minaei, E. Yuce, and O. Cicekoglu, "A versatile active circuit for realizing floating inductance, capacitance, FDNR and admittance converter," *Analog Integrated Circuits and Signal Processing,* vol. 47, no. 2, pp.199–202, 2006.

[2] K. Pal, "New inductance and capacitor floatation schemes using current conveyors," *Electronics Letters*, vol.17, no. 21, pp. 807–808, 1981.

[3] P. V. Ananda Mohan, "Floating capacitance simulation using current conveyors," *Journal of Circuits Systems and Computers,* vol. 14, no. 1, pp. 123-128, 2008.

[4] P. Mongkolwai, T. Pukkalanun and W. Tangsrirat, "Electronically tunable floating capacitance simulator with only VDTAs and a grounded capacitor," *4th International Science, Social Science, Engineering and Energy Conference- 2012.*

[5] A. Lahiri, "DO-CCII based generalised impedance convertor simulates floating inductance, capacitance multiplier and FDNR," *Australian Journal of Electrical & Electronics Engineering*, vol. 7, no. 1, 2010.

[6] R. Senani "Realization of liner voltage controlled resistance in floating form," *Electronics letters*, vol. 30, no. 23, pp. 1909-1910, 1994.

[7] V. Riewruja and W. Petchmaneelumka, " Floating current controlled resistance converters using OTAs" *International Journal of Electronics and Communications-AEU*, vol. 62, no. 10, pp. 725-731, 2008.

[8] E. Yuce, "On the implementation of the floating simulators employing a single active device," *International Journal of Electronics and Communications-AEU*, vol. 61, no. 7, pp. 453-458, 2007.

[9] E. Yuce, O. Cicekoglu and S. Minaei, "CCII-Based Grounded to Floating Immittance Converter and a Floating Inductance Simulator" *Analog Integrated Circuits and Signal Processing*, vol. 46, no. 3, pp. 287–291, 2006

[10] S. Minaei, E. Yuce and O. Cicekoglu, "A versatile active circuit for realizing floating inductance, capacitance, FDNR and admittance converter," *Analog Integrated Circuits and Signal Processing*, vol. 47, no. 2, pp.199–202, 2006.

[11] R. A. Saad and A. M. Soliman, "On the systematic synthesis of CCII-based floating simulators," *International Journal of Circuit Theory and Applications*, vol. 38, no. 9, p. 935 – 967, 2010.

[12] M. Kumngern, U. Torteanchai and K. Dejhan "Voltage controlled floating resistor using DDCC," Radioengineering, vol. 20, no. 1, pp. 327–333, 2011.

[13] E. Yuce, S. Minaei and O Cicekoglu, "Resistorless floating immitance function simulators employing current controlled conveyors and a grounded capacitor," *Electrical Engineering*., vol. 88, no. 6, pp. 519-525, 2006.

[14] M. Sagbas, U. E. Ayten, H. Sedef and M. Koksal, "Floating immittance function simulator and its applications," *Circuits Systems and Signal Processing*, vol. 28, no. 1, pp. 55-63, 2009.

[15] U. E. Ayten, M. Sagbas, N. Herencsar and J. Koton, "Novel Floating General Element Simulators Using CBTA," *Radioengineering,* vol. 21, no. 1,pp. 11-19, 2012

[16] M. Sagbas "Component reduced floating±L,±C and±R simulators with grounded passive components," *International Journal of Electronics and Communications-AEU*, vol. 65, no. 10, pp. 794-798, 2011.

[17] Y. Li, "A series of new circuits based on CFTAs," *International Journal of Electronics and Communications-AEU*, vol. 66, no.7, pp. 587-592, 2012.

[18] E. Yuce, "A novel floating simulation topology composed of only grounded passive components," *International Journal of Electronics*, vol. 97, no. 3, pp. 249–262, 2010.

[19] D. Biolek, R. Senani, V. Biolkova and Z. Kolka, "Active elements for analog signal processing; classification, review and new proposals," *Radioengineering*, vol. 17, no. 4, pp. 15-32, 2008.

[20] A. Yesil, F. Kacar and H. Kuntman, "New simple CMOS realization of voltage differencing transconductance amplifier and its RF filter application," *Radioengineering,* vol. 20, no. 3, pp. 632-637, 2011.

[21] D.Prasad, D. R. Bhaskar and M. Srivastava, "Universal Current-Mode Biquad Filter using a VDTA," *Circuits and Systems*, vol. 4, no. 1, pp. 32-36, 2013.

[22] D. Prasad, D. R. Bhaskar and M. Srivastava, "Universal voltage-mode biquad filter using voltage differencing transconductance amplifier," *Indian Journal of Pure and Applied Physics*, vol. 51, no. 12, pp. 864-868, 2013.

[23] D. Prasad, M. Srivastava and D. R. Bhaskar, "Transadmittance - type universal current-mode biquad filter using voltage differencing transconductance amplifiers," *International Scholarly Research Notices*, 4 pages, 2014.

[24] D. Prasad, M. Srivastava and D. R. Bhaskar, "Electronically controllable fully uncoupled explicit current mode quadrature oscillator using VDTA and grounded capacitors," *Circuits and Systems*, vol. 4, no. 2, pp. 169-172, 2013.

[25] M. Srivastava, D. Prasad and D. R. Bhaskar, "New Parallel R-L impedance using single VDTA & its high pass filter applications," *In Proc. of International Conference on Signal Processing and Integrated Networks-2014(SPIN-2014),*Noida, pp. 535-537, 2014.