

# CFOA-Based Fractional Order $PI^{\lambda}D^{\delta}$ Controller

Tada Comedang and Pattana Intani

**Abstract**— Conventional Current Feedback Operational Amplifier (CFOA) is not current controllable or not electronically controllable. It is thus of interest to add a current mirror into the CFOA in order to make it current controllable. This modification can be achieved by using Diamond Transistor (DT) instead of going through complicated IC fabrication process. This work applies the modified CFOA in fractional-order proportional integral derivative ( $PI^{\lambda}D^{\delta}$ ) controller. Both simulation and experimental results confirm that the modified CFOA is electronically controllable.

**Index Terms**— CFOA, Fractional-order proportional integral derivative.

Original Research Paper  
DOI: 10.7251/ELS1721025C

## I. INTRODUCTION

SEVERAL active elements for analogue signal processing have recently been proposed. Some applications of these components have been given in the literature, for example, differentially buffered transconductance amplifiers (DBTAs) [1], current differencing transconductance amplifiers (CDTAs) [2], current follower transconductance amplifiers (CFTAs) [3], current conveyor transconductance amplifiers (CCTAs) [4-8], differential difference current conveyor (DDCC) [9-10] and others. Unfortunately, for the most part, development of the applications will be done via a simulation program with a transistor model of the active components of some bipolar or CMOS technology where practical usability is questionable. Attributable, experimental verification via their on-chip fabrication is expensive and time-consuming [11].

Among the mentioned active elements, the current feedback operational amplifier (CFOA) is an interesting active component, especially suitable for a class of analogue signal processing [12-14]. This device can operate in both current and voltage modes, provides flexibility and enables a variety of circuit designs. In addition, it can offer advantageous

features, such as high slew rate, freedom from parasitic capacitances, wide bandwidth and simple implementation [15-18].

Nowadays, the CFOA can be found commercially, for example, the AD844 from Analog Devices Inc. [13]. However, the CFOA cannot be controlled by the electronic controllability of the hysteresis of the output signal. The electronic control method has become more popular more than those by passive elements (i.e., resistors and capacitors) due to how it can easily be adapted to automatic or microcontroller-based controls. Diamond transistors (DT) are readily available commercially (commercially marked OPA 860) [19] and belong to the group of well-known commercial products commonly used for wide-bandwidth systems, including high performance video, RF and IF circuitry. It includes a wideband, bipolar operational transconductance amplifier (OTA) and voltage buffer amplifier. The transconductance of the OPA860 can be adjusted with an electronic control, allowing bandwidth, quiescent current, and gain trade-offs to be optimized. Used as a basic building block, the OPA860 simplifies the design of AGC amplifiers, LED driver circuits for fibre optic transmission, integrators for fast pulses, and fast control loop amplifiers and control amplifiers for capacitive sensors and active filters. Concrete experiments have led to the observation that the OPA860 is a useful element for analogue signal processing in the frequency range of units and tens of wide bandwidth.

Proportional integral derivative (PID) control has been adopted in many engineering applications [20-22]. Recently, several literature reviews have studied mechanical systems described by fractional-order state equations [23-25], i.e., equations involving so-called fractional derivatives and integrals [26-28]. A fractional-order  $PI^{\lambda}D^{\delta}$  controller, first proposed by Podlubny, is a generalization of a PID controller, involving an integrator of order and a differentiation of order [29]. Expanding derivatives and integrals to fractional orders can adjust a control system's frequency response directly and continuously. This great flexibility makes it possible to design more robust control systems [30]. Several methods have been reported for fractional-order  $PI^{\lambda}D^{\delta}$  design. At the present time, there are numerous methods for the approximation of fractional derivatives and integrals, and fractional calculus can be easily used in a wide variety of applications (e.g. control theory, new fractional controllers, system models, electrical circuits theory, fractances, capacitor theory, etc.) [31-49].

Existing evidence has confirmed that the best fractional-

Manuscript received 15 December 2015. Received in revised form September 14, 2016. Accepted for publication December 28, 2016.

T. Comedang is with the Faculty of Electrical Engineering, Pathumwan Institute of Technology, Bangkok, Thailand (phone: +668-24-520-041; e-mail: tada-comedang@hotmail.com).

P. Intani is with the Faculty of Electrical Engineering, Pathumwan Institute of Technology, Bangkok, Thailand (pattana@pit.ac.th).

order controller can outperform the best integer-order controller. It has also been answered in the literature why fractional-order control should be considered even when integer (high)-order control works comparatively well [50-51]. Fractional-order  $PI^{\lambda}D^{\delta}$  controller tuning has reached a matured state of practical use. Because (integer-order) PID control dominates the industry, we believe that fractional-order  $PI^{\lambda}D^{\delta}$  will gain increasing impact and wide acceptance. Furthermore, we also believe that, based on some real world examples, fractional-order control is ubiquitous when the dynamic system is of a distributed parameter nature [52].

In this paper, the conception of this active element for experimental purposes is built from commercially available devices. There is the diamond transistor and a wideband voltage buffer designed (OPA860) for positive and negative W terminals. Note that the manufactured CFOA [53] does not provide this feature. It is necessary to have two positive current outputs for the proposed fractional-order  $PI^{\lambda}D^{\delta}$ . The CFOA is applied for fractional-order  $PI^{\lambda}D^{\delta}$  design. To match the criteria of industrial applications, the best fractional-order controller can outperform the best integer-order controller. Similarly, a circuit exhibiting fractional-order behaviour is called a fractance. The design of fractances can be performed easily using any of the rational approximations or a truncated continued fraction expansion (CFE), which also gives a rational approximation. Generally speaking, there are three basic fractance devices. The most popular is a domino ladder circuit network. Very often used is a tree structure of electrical elements [54]. Therefore, fractional-order  $PI^{\lambda}D^{\delta}$  causes the result  $0 < \lambda, \delta \leq 1$ , and the fractional order is approximated using a fractance circuit.

## II. CFOA ELEMENT BASED ON OPA860

In Fig. 1, the schematic symbol of the CFOA, which was given in the paper [53], has been shown with an additional output terminal of  $W^-$ , which is the negative of the  $W$  terminal. The proposed behavioural model of the CFOA is given in Fig. 1, where  $Y$  and  $X$  are input terminals and  $Z$ ,  $W$ , and  $W^-$  are output terminals. Its definition is shown in the matrix as follows (1):

$$\begin{bmatrix} V_X \\ V_Y \\ I_Z \\ V_{W^+} \\ V_{W^-} \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1/g_{m1} & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & g_{m2} & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_Y \\ V_Z \\ I_{W^+} \\ I_{W^-} \end{bmatrix}, \quad (1)$$

where  $g_m$  represents the transconductance gain of the CFOA. For a CFOA implemented with OPA860,  $g_m$  can be

$$g_{m1} = \frac{1}{R_X + (1/I_{Q1})}, \quad (2)$$

$$g_{m2} = \frac{R_L}{R_E + (1/I_{Q2})}. \quad (3)$$

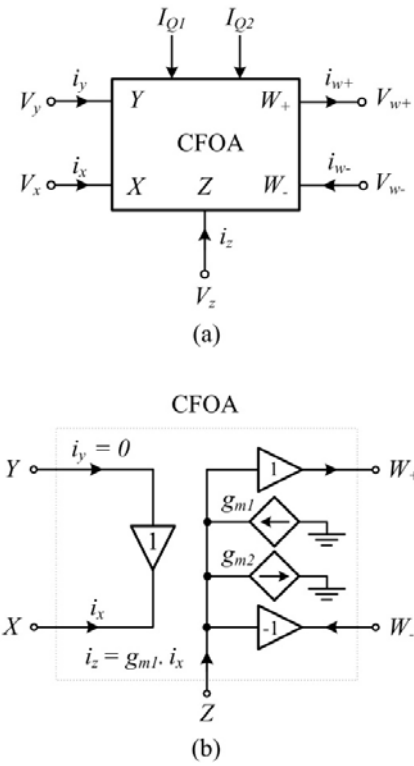


Fig. 1. CFOA elements' circuit symbol. (a) schematic symbol (b) equivalent circuit.

From the advantage already mentioned in the introduction, CFOA can be constructed from commercially available devices, as is shown in Fig. 2. It consists of the diamond transistors (OPA 860), where  $g_m$  represents the amplifier gain of the CFOA for a negative  $W$  terminal ( $W^-$ ) implemented with diamond transistors. In this paper, the idea to develop the features of the CFOA is increased by using the Buffer of OPA860, which can be useful in the work for the proposed FO-PID voltage mode.

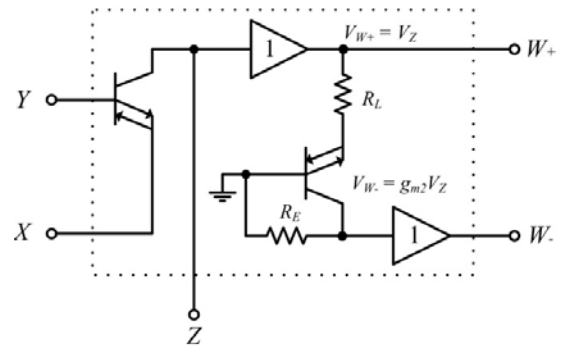


Fig. 2. The CFOA using commercially available devices numbers OPA 860.

The principle negative  $W$  terminal of CFOA. Fig. 3 through Fig. 8 show the main features obtained by simulations of the CFOA element shown in Fig. 2. The result presented in Fig. 3 is that the voltage transfer between the  $Y$  and  $X$  ports of the proposed CFOA is approximately 185 MHz, and current transfers between the  $X$  and  $Z$  ports being approximately 81 MHz is shown in Fig. 4. The simulation results lead to the

observation that the CFOA is a useful element for the frequency range of units and tens of megahertz (MHz). Later, Fig. 5 through Fig. 8 show the DC transfer characteristic between the Z and W+ ports. It also shows the DC transfer characteristic between the Z and W- ports. This transconductance gain can be controlled by the bias current  $I_{Q1}$  and adjust the gain adjustable resistor ( $R_L$ ) from  $100\ \Omega$  to  $500\ \Omega$ , and  $I_{Q2} = 11.2\ \text{mV}$ . The results presented show high linearity input voltage (Z) from -4 to 4 volts.

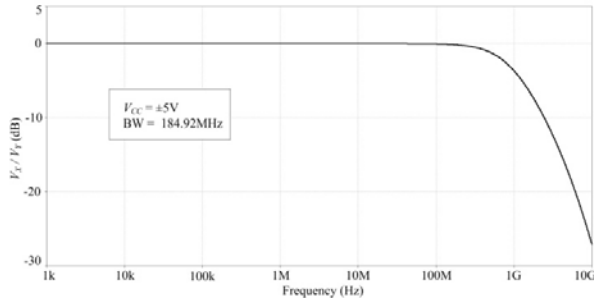


Fig. 3. Voltage transfer between the Y and X ports of CFOA.

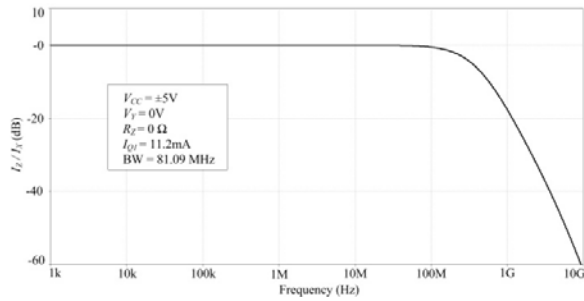


Fig. 4. Current transfers between the X and Z ports of CFOA.

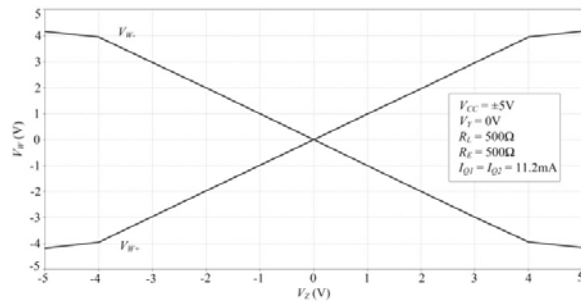


Fig. 5. DC transfer characteristic between the Z and W ports.

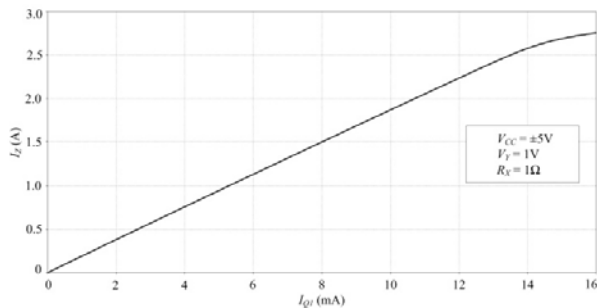


Fig. 6. DC transfer characteristic of the Z port while adjusting the transconductance gain of  $I_{Q1}$ .

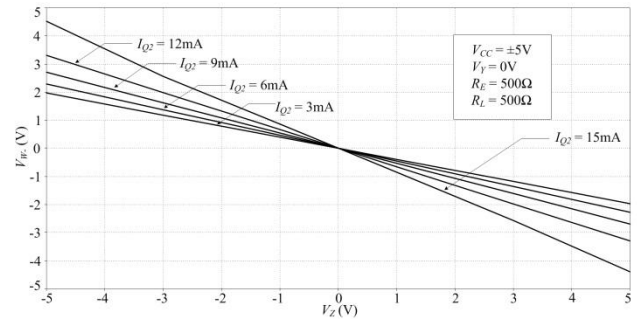


Fig. 7. DC transfer characteristic between the Z and W- ports while adjusting the transconductance gain of  $I_{Q2}$ .

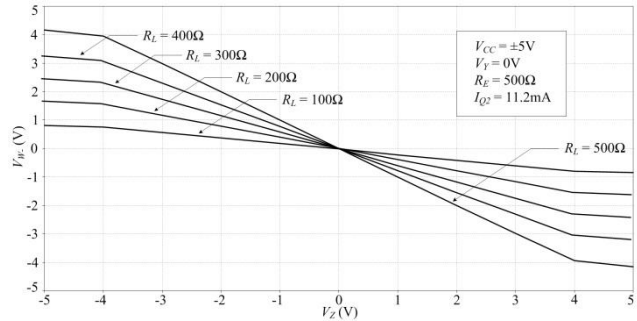


Fig. 8. DC transfer characteristic between the Z and W- ports while adjusting the gain adjustable  $R_L$ .

Results suitable for applications in practice bases for proportional integral derivative (PID) were introduced in some recent works, replacing offers by simulation programs with transistor models of active components of some bipolar or CMOS technology. The above designs of topologies of CFOA for analogue signal processing useful wide band up the prototyping most applications of special active elements, which are not currently available on the chip.

### III. CFOA FRACTIONAL-ORDER PID

The design realisation and performance of the fractional-order  $PI^{\lambda}D^{\delta}$  controller have been presented. The fractional-order  $PI^{\lambda}D^{\delta}$  is constructed using two circuits exhibiting fractional order behaviour, called a fractance [54] of orders  $\lambda$  and  $\delta$  ( $0 < \lambda, \delta \leq 1$ ). The most popular is a domino ladder circuit network [55-56]. However, from the results of study in earlier research, resistors and capacitors are untraceable on the market [57-62]. Therefore, this research will focus the design in accordance with market aplikasi that actually works. In this section, a comparison of integer-order PID and fractional-order  $PI^{\lambda}D^{\delta}$  is made using PSPICE and by practical experimentation.

#### A. Analogue Realization: Fractance Circuits (domino ladder circuit network)

The design of fractances can be performed easily using the rational approximations, which also give a rational approximation. The relationship between the finite domino ladder network, shown in Fig. 9, and the continued fraction (4) provides an easy method for designing a circuit with a given impedance  $Z(s)$ .

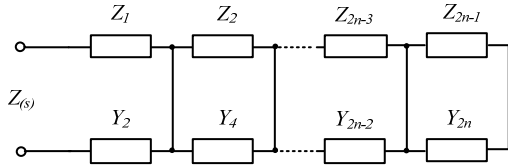


Fig. 9. Finite domino ladder network.

Let us consider the circuit depicted in Fig. 9, where  $Z_{2k-1}(s)$  and  $Y_{2k}(s)$ ,  $k = 1, \dots, n$ , are given impedances of the circuit elements. The resulting impedance  $Z(s)$  of the entire circuit can be found easily if we consider it in the right-to-left direction [31,37]:

$$Z(s) = Z_{1(s)} + \frac{1}{Y_{2(s)} + \frac{1}{\dots \frac{1}{Y_{2n-2(s)} + \frac{1}{Z_{2n-1(s)} + \frac{1}{Y_{2n(s)}}}}}} \quad (4)$$

The rational approximation of the fractional integrator/differentiator can be formally expressed as:

$$s^{\pm\alpha} \approx \left\{ \frac{P_p(s)}{Q_q(s)} \right\}_{p,q} = Z(s), \quad (5)$$

where  $p$  and  $q$  are the orders of the rational approximation and  $P$  and  $Q$  are polynomials of degree  $p$  and  $q$ , respectively.

The rational approximation of the fractional integrator/differentiator can be formally expressed as:

$$Z(s) = R_1 + \frac{1}{C_{1(s)}} \frac{1}{R_2} \frac{1}{C_{2(s)}} \frac{1}{R_3} \frac{1}{C_{3(s)}} \frac{1}{R_4} \frac{1}{C_{4(s)}} \frac{1}{R_5} \frac{1}{C_{5(s)}}, \quad (6)$$

If we consider that  $Z_{2k-1} \equiv R_{k-1}$  and  $Y_{2k} \equiv C_{k-1}$  for  $k = 1, \dots, n$  in Fig. 9, then the values of the resistors and capacitors of the network are chosen as  $R_1=51\Omega$ ,  $R_2=535\Omega$ ,  $R_3=5.6k\Omega$ ,  $R_4=13k\Omega$ ,  $R_5=820k\Omega$ ,  $C_1=470pF$ ,  $C_2=820pF$ ,  $C_3=3.9nF$  and  $C_4=820pF$ .

Therefore, the direct calculation of circuit elements was proposed. The impedance of the domino ladder circuit network (or transmission line) can be written as:

$$Z(s) = \frac{1}{(0.8 \times 10^{-9})s^{0.2}} \quad (7)$$

where  $0.8 \times 10^{-9}$  is independent of the angular frequency and  $\alpha = 0.2$ .

To demonstrate the performance of the proposed domino ladder circuit network, the measured prototype used is shown in Fig. 10.

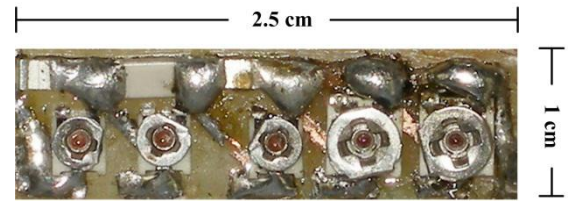


Fig. 10. The measured prototype domino ladder circuit network.

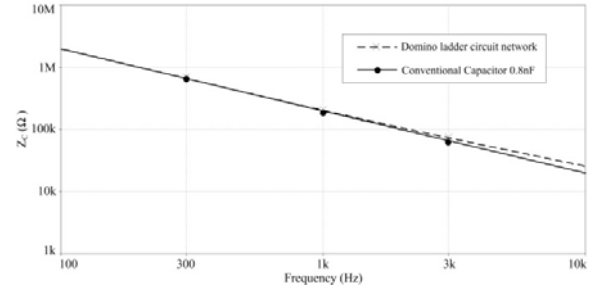


Fig. 11. Magnitude of the input impedance of the domino ladder circuit network compared to that of a conventional capacitor.

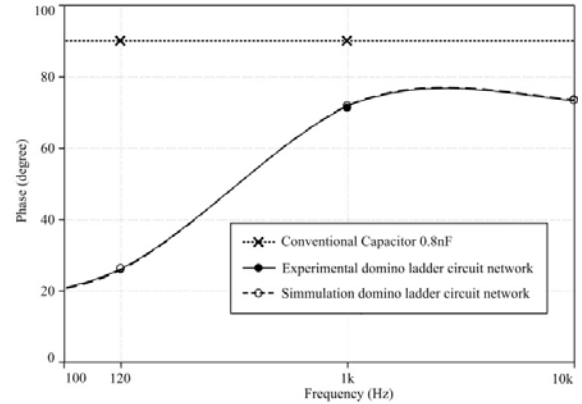


Fig. 12. Phase experiment of the frequency variations of the domino ladder circuit network compared to simulation.

From the simulation and experimental results in Fig. 11 and Fig. 12, the Magnitude and Phase of the domino ladder circuit network are compared to those of a conventional capacitor. The results confirm that the domino ladder circuit network characteristics presented work correctly from a theoretical perspective.

### B. Synthesis of proposed fractional-order $PI^{\alpha}D^{\beta}$ employing CFOA

A fractional-order  $PI^{\alpha}D^{\beta}$  controller is composed of proportional fractional-order integral and fractional-order derivative terms. The proposed fractional-order  $PI^{\alpha}D^{\beta}$  controller employs three CFOA, a grounded domino ladder circuit network ( $Z(s)$ ) and resistors as shown in Fig. 13. The transfer function of fractional-order  $PI^{\alpha}D^{\beta}$  can be written as:

$$T(s) = \frac{V_{out}(s)}{V_{in}(s)} = K_p + \frac{K_i}{s^{\alpha 1}} + s^{\alpha 2} K_d, \quad (8)$$

$$T(s) = \frac{s^{\alpha 1 + \alpha 2} K_d + s^{\alpha 1} K_p + K_i}{s^{\alpha 1}}. \quad (9)$$

Here, the proportional constant,

$$K_p = \frac{g_{m2}R_2R_8}{g_{m1}R_1R_5}, \quad (10)$$

the integral constant,

$$K_i = \frac{g_{m4}R_8}{g_{m3}R_3R_6Z_1s^{\alpha_1}}, \quad (11)$$

and the derivative constant,

$$K_d = \frac{g_{m6}R_4R_8Z_2s^{\alpha_2}}{g_{m5}R_7}, \quad (12)$$

The transfer function of the fractional-order  $PI^{\alpha}D^{\beta}$  controller is given by

$$T(s) = \frac{g_{m2}R_2R_8}{g_{m1}g_{m7}R_1R_5} + \frac{g_{m4}R_8}{g_{m3}g_{m7}R_3R_6Z_1s^{\alpha_1}} + \frac{g_{m6}R_4R_8Z_2s^{\alpha_2}}{g_{m5}g_{m7}R_7}, \quad (13)$$

where  $g_{m(\text{odd number})}$  is shown in (2) and  $g_{m(\text{even number})}$  is shown in (3), respectively.

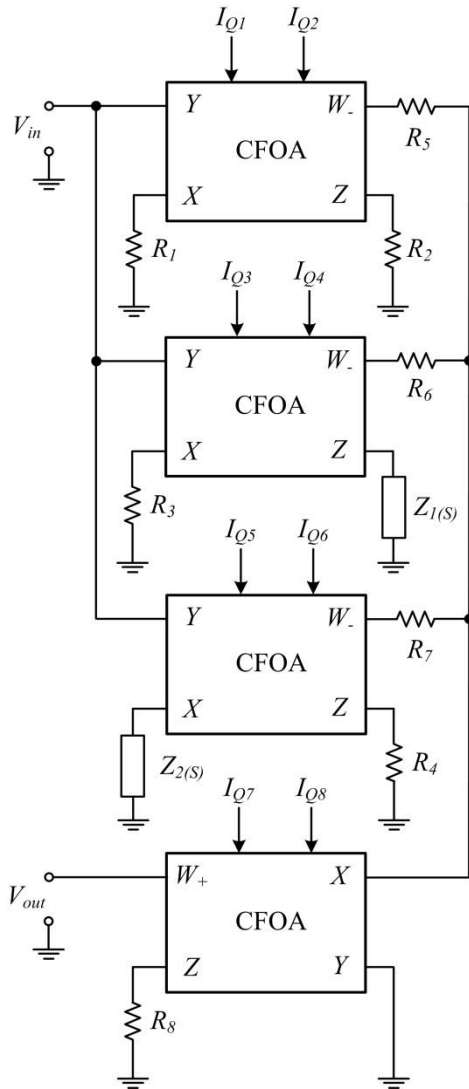


Fig. 13. Analogue fractional order  $PI^{\alpha}D^{\beta}$  controller.

From (13), the controller's parameters can be assigned to the required values by adjusting the corresponding resistor. Additionally, it can be seen that the fractional-order  $PI^{\alpha}D^{\beta}$  parameters ( $K_p$ ,  $K_i$  and  $K_d$ ) can be independently electronically controlled by the current transfers  $I_{Q1}$ - $I_{Q6}$ , respectively.

#### IV. SIMULATION AND EXPERIMENTAL RESULTS

In this section, a comparison of integer-order PID and fractional-order  $PI^{\alpha}D^{\beta}$  is made using the PSPICE simulation program and by practical experimentation. To prove the performances of the proposed controllers, the Diamond transistors (DT) employed in CFOA of the proposed circuit were simulated and experimented with by using the commercially available OPA 860. Fig. 2 depicts a schematic description of the internal construction of the CFOA.

Fig. 13 depicts an analogue implementation of a fractional-order  $PI^{\alpha}D^{\beta}$  controller. A fractional-order integrator is approximated by the domino ladder circuit network impedance  $Z_1(s)$ , and fractional-order differentiator is approximated by the impedance  $Z_2(s)$ , where orders of both approximations are  $\alpha = 0.2$ . In this case, if we use identical resistors (R-series) and identical capacitors (C-shunt) in the domino ladder circuit network, then the behaviour of the circuit will be that of a fractional-order integrator/differentiator. Realization and measurements of such types of controllers were done in this paper.

The transfer function of the fractional-order  $PI^{\alpha}D^{\beta}$  controller can be evaluated and rewritten as a fractional order:

$$T(s) = \frac{V_{out}(s)}{V_{in}(s)} = K_p + \frac{K_i}{s^{0.2}} + s^{0.2}K_d, \quad (14)$$

$$T(s) = \frac{s^{0.4}K_d + s^{0.2}K_p + K_i}{s^{0.2}}. \quad (15)$$

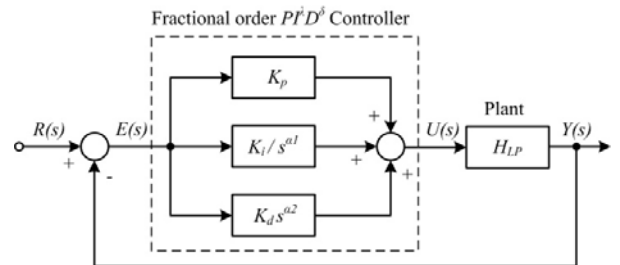


Fig. 14. Fractional-order  $PI^{\alpha}D^{\beta}$ -controlled System.

To validate the practical application of the proposed controller, a passive low-pass filter was used to realize a closed-loop control system, as depicted in Fig. 14. For the low-pass filter, the circuit shown in Fig. 15 with an addition output terminal is chosen. The transfer function of the 2<sup>nd</sup>-order Sallen-Key Low-pass filter can be written as:

$$H_{LP} = \frac{V_{out}}{V_{in}} = \frac{1}{R_1R_2C_1C_2} \frac{1}{s^2 + s\left(\frac{1}{R_2C_1} + \frac{1}{R_1C_1}\right) + \frac{1}{R_1R_2C_1C_2}}, \quad (16)$$

This Sallen-Key low-pass filter has the following transfer function with the values of  $R_1=30\text{ k}\Omega$ ,  $R_2=18\text{ k}\Omega$ ,  $C_1=10\text{ nF}$  and  $C_2=4.7\text{ nF}$ . Therefore, direct calculation of circuit elements was proposed. The Sallen-Key low-pass filter can be written as:

$$H_{LP} = \frac{V_{out}}{V_{in}} = \frac{39401103.23}{s^2 + s8888.89 + 39401103.23} \quad (17)$$

From (15), the  $R$  and  $C$  values for the Sallen-Key low-pass filter can be calculate at a given cut-off frequency ( $f_c$ ), quality factor ( $Q$ ) and Damping ratio ( $\zeta$ ) as follows:  $f_c = 1\text{ kHz}$ ,  $Q = 0.7$ , and  $\zeta = 0.7$ .

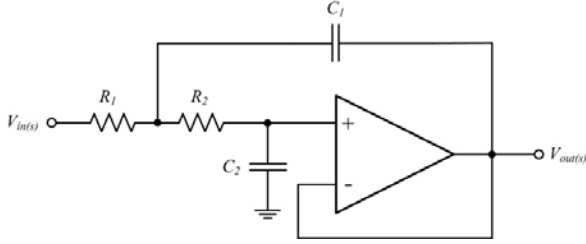


Fig. 15. Sallen-Key Active Filter.

#### A. Comparison in Simulation

To demonstrate the performance of the proposed fractional-order  $PI^{\delta}D^{\delta}$  controller, the PSPICE simulation program was used for the examinations. The CFOAs of the proposed fractional-order  $PI^{\delta}D^{\delta}$  controller were simulated by using the domino ladder circuit network from (7) to achieve the behaviour of the circuit as a fractional-order integrator/differentiator. For the proposed fractional-order  $PI^{\delta}D^{\delta}$  controller, PSPICE simulations are performed with  $R_1=R_5=R_6=R_7=R_8=100\ \Omega$ ,  $R_2=200\ \Omega$ ,  $R_3=200\text{ k}\Omega$ ,  $R_4=100\text{ k}\Omega$ ,  $Z_1(s)=Z_2(s)=1/[(0.8 \times 10^{-9})s^{0.2}]$ , and  $I_{Q1}=I_{Q2}=I_{Q3}=I_{Q4}=I_{Q5}=I_{Q6}=11.2\text{ mA}$  for the circuits depicted in Fig. 13. Therefore, the fractional-order  $PI^{\delta}D^{\delta}$  controller has the parameters that are calculated as  $K_p=1.06 \times 10^3$ ,  $K_i=662.50 \times 10^6$ , and  $K_d=42.24 \times 10^{-3}$ . These proposed circuits were biased with the symmetrical  $\pm 5\text{ V}$  supply voltages.

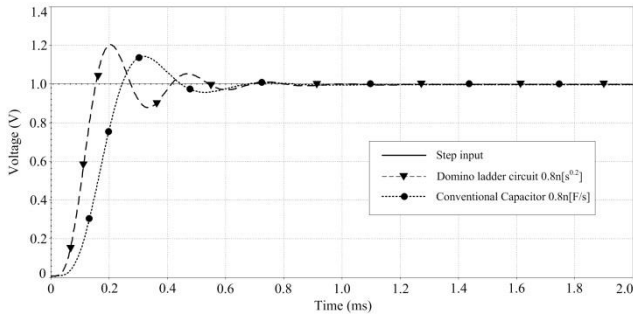


Fig. 16. Step response for PID and open-loop systems.

In Fig. 16, the fractional-order  $PI^{\delta}D^{\delta}$  controller is compared with integer-order PID. From Fig. 16, we can see that the overshoot of the unit step response with an open loop using the designed fractional-order  $PI^{\delta}D^{\delta}$  controller is much shorter than that using the designed integer-order PID controller.

A closed-loop control system depicted in Fig. 14 can be constructed with the fractional-order  $PI^{\delta}D^{\delta}$  controller in Fig. 13 and the Sallen-Key low-pass filter with the transfer function given in (16). The simulated response for this fractional-order  $PI^{\delta}D^{\delta}$  controller with unit step is given in Fig. 17. It is observed that the proposed fractional-order  $PI^{\delta}D^{\delta}$  controller system enters steady-state and follows the unit step input with a steady-state error compared with integer-order PID.

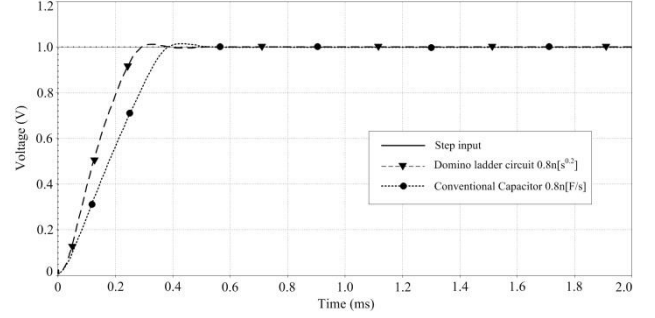


Fig. 17. Closed-loop response of the system.

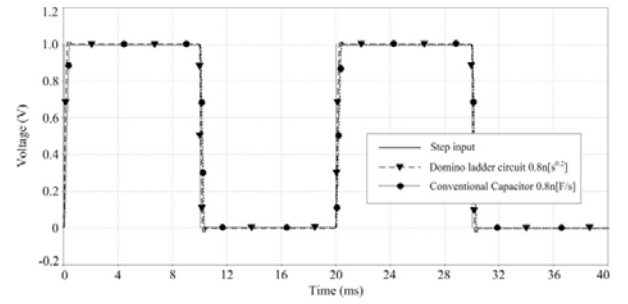


Fig. 18. Real-time closed-loop response of system.

For controlled system performance comparison, we have summarized some performance characteristics in Table 1 for the controlled system with both controllers. In any controlled system, the final step in the design process is the real-time controlled experiment. As can be observed from Fig. 18, the performances of the controllers are confirmation of the simulation results based on the identified model.

TABLE I  
SIMULATION RESULTS OF THE PSPICE-BASED CONTROL SALLEN-KEY ACTIVE LOW-PASS FILTER

Parameters	Fractional order $PI^{\delta}D^{\delta}$ controlled	Integer order PID controlled
Max. overshoot	2.24%	2.36%
Rise time	234.37 $\mu\text{s}$	324.72 $\mu\text{s}$
Settling time	269.06 $\mu\text{s}$	445.43 $\mu\text{s}$
Steady-state error	553.66 $\mu\text{s}$	654.49 $\mu\text{s}$

From Fig. 16 to Fig. 18, we can see that the overshoot, rise time, settling time and steady-state error of the unit step response using the designed fractional-order  $PI^{\delta}D^{\delta}$  controller is much shorter than that using the designed integer-order PID controller. Thus, following our proposed design algorithms, the fractional-order  $PI^{\delta}D^{\delta}$  controller outperforms the integer-

order PID for the fractional-order systems considered.

*B. Experimental Verification in real-time*

A closed-loop control system prototype is shown in Fig. 19. The passive and active elements are the same as appeared in the simulation program. The responses of fractional-order  $PI^{\delta}D^{\delta}$  and integer-order PID controllers are compared via the experimental setup of the control system. Fig. 20 and Fig. 21 show responses of fractional-order  $PI^{\delta}D^{\delta}$  and integer-order PID controllers per unit step. Fig. 22 and Fig. 23 show the real-time closed-loop response of the system for both the controllers.

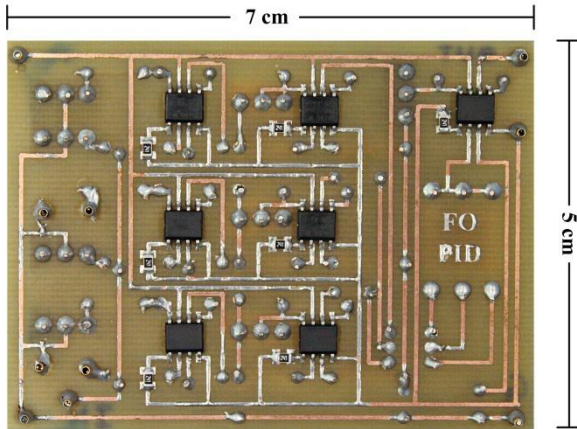


Fig. 19. The measured fractional order  $PI^{\delta}D^{\delta}$  prototype.

TABLE II  
EXPERIMENTAL RESULTS OF THE CIRCUIT PROTOTYPE-BASED CONTROL  
SALLEN-KEY ACTIVE LOW-PASS FILTER

Parameters	Fractional order $PI^{\delta}D^{\delta}$ controlled	Integer order PID controlled
Max. overshoot	8.11%	12.17%
Rise time	172.50 $\mu$ s	202.90 $\mu$ s
Settling time	490 $\mu$ s	950 $\mu$ s
Steady-state error	750 $\mu$ s	1.25 ms

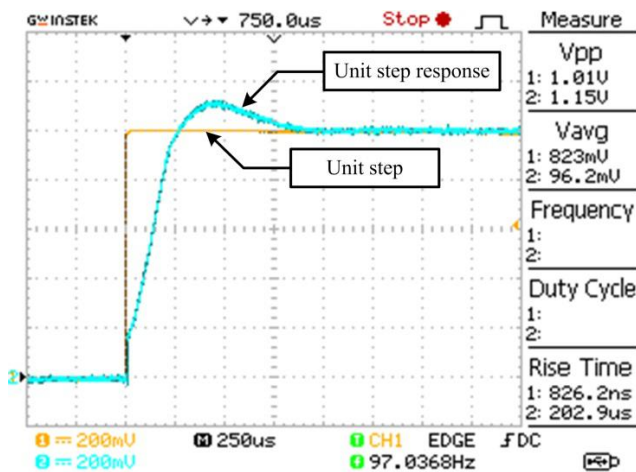


Fig. 20. Real-time closed-loop response of the Integer-order system.

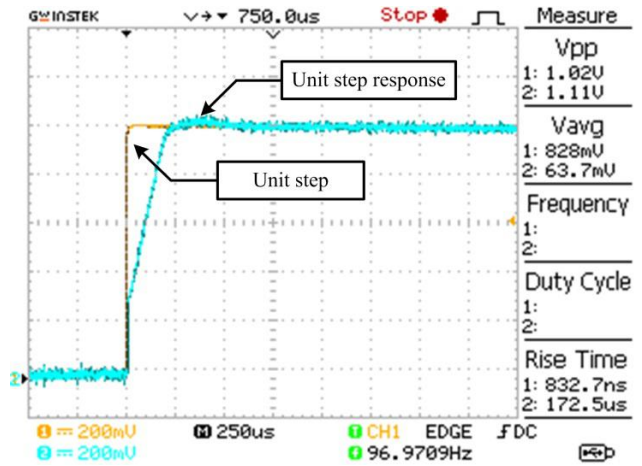


Fig. 21. Real-time closed-loop response of the Fractional-order system.

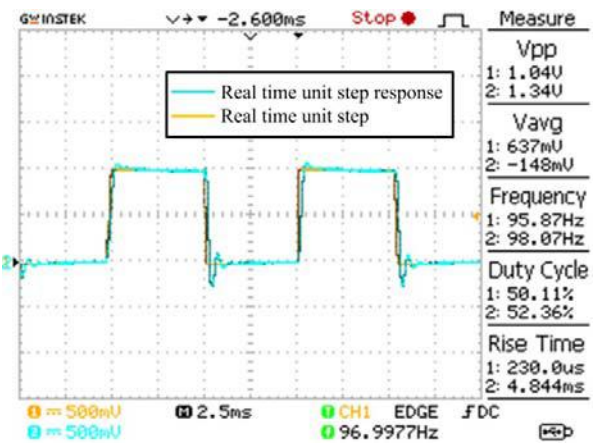


Fig. 22. Real-time closed-loop response of the Integer-order system.

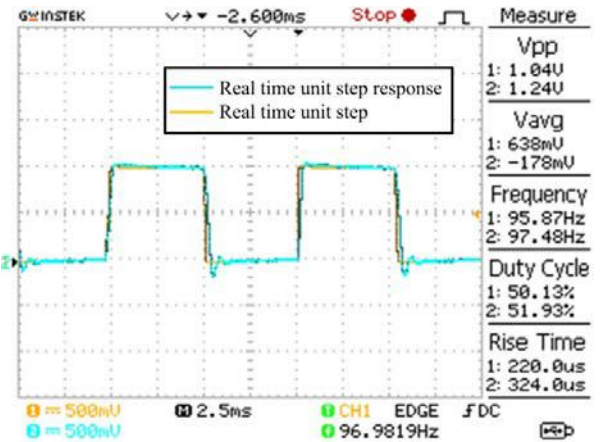


Fig. 23. Real-time closed-loop response of the Fractional-order system.

For control system performance enhancement comparison, we have summarized some performance characteristics in Table 2 for the feedback control system with both controllers. As seen, the experimental results confirm the theoretical results very well.

## V. CONCLUSION

The modified version of the building block, the so-called current feedback operational amplifier (CFOA), has been introduced in this paper. This modification can be achieved by using Diamond Transistor (DT) instead of going through complicated IC fabrication process. Modification of the CFOA has been applied as a fractional-order proportional integral derivative ( $PI^{\delta}D^{\delta}$ ) controller. In this CFOA application, two fractional-order proportional integral controllers have been designed to improve the performance of fractional-order systems, which can model many real systems in control engineering. Comparisons have been made between the fractional-order proportional integral controllers and the traditional integer-order PID controller. From the simulation and experimental results, we can see that the overshoot, rise time, settling time and steady-state error of the unit step response using the designed fractional-order  $PI^{\delta}D^{\delta}$  controller is much shorter than that using the designed integer-order PID controller.

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