A Novel Domino Logic with Modified Keeper in 16nm CMOS Technology

Smita Singhal, Anu Mehra, and Upendra Tripathi

***Abstract*—Domino logic is a clocked CMOS (*Complementary Metal-Oxide Semiconductor*) logic with fewer transistors than static CMOS logic. A PMOS (P-type Metal-Oxide Semiconductor) transistor, known as "keeper", is included in the design to improve the noise tolerance performance and to reduce the leakage current. The aspect ratio i.e. W/L of the keeper (W=width and L=length) is kept low for the correct functionality of the domino logic. This paper proposes a domino logic with modified keeper in order to improve the circuit with respect to power and area as compared to various existing techniques of domino logic i.e. *clock delayed domino logic* (CDD), *high speed domino logic* (HSD), *multi threshold high speed domino logic* (MHSD), *clock delayed sleep mode domino logic* (CDSMD), *sleep switch domino logic* (SSDD), *PMOS* only sleep switch domino logic (PSSDD), *reduced delay variations domino logic* (RDVD) and *Foot Driven Stack Transistor Domino Logic* (FDSTDL). The proposed as well as existing domino logics, for 8-input as well as 16-input OR gate in 16nm CMOS technology, are simulated for different values of W/L of keeper with W/L ratio ranging from 1 to 6. The *power-delay-product*(PDP) of proposed design has improved as compared to the existing designs. For 8-input OR gate and W/L=6, PDP had improved to maximum of 99.99% for CDD and minimum of 38.09% for SSDD.**

***Index Terms*—Domino, dynamic, static power, CMOS, keeper.**

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I. Introduction

With the growing trend of wireless communication and portable computing, power dissipation has become one of the critical factors in the development of semiconductor industry. The number of transistors on an integrated circuit are continously growing according to Moore's law [1]. Examples are latest cell phone application processors. The transistor count has increased from 1 billion transistors in processor A5 to 2 billions in processor A6 and then to 3 billion in processor A6X [2]. To meet this high transistor density and to increase the performance, CMOS (*Complementary Metal-Oxide Semiconductor*) technology has to continue to scale. Technology scaling has lead to shrinking of parameters like supply voltage, threshold voltage, gate oxide thickness in order to increase the performance of the circuit [3]. But this has resulted in higher power dissipation. Minimizing power dissipation calls for conscious effort at each abstraction level and at each phase of design process [4].

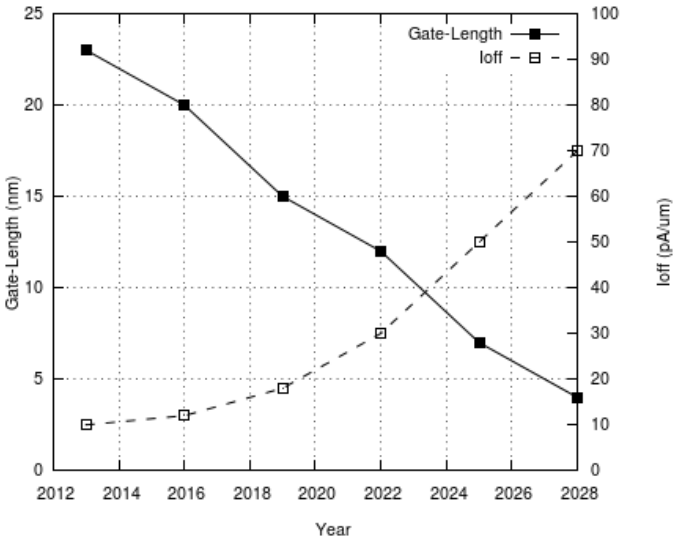

Fig. 1. Trends of changes in gate-length and I_{off} according to ITRS 2013.

The power dissipation in a CMOS circuit comprises of mainly two components – dynamic power and static power. Dynamic power occurs due to the switching activities of circuits i.e. charging and discharging of load capacitances, short-circuit current from supply voltage to ground and glitches in the output waveforms. Static power dissipation is related to the logical state of the circuit rather than the switching activities. In CMOS circuits, static power dissipation occurs due to leakage current that flows when the inputs, and thus the outputs, of the gate are not changing. Fig. 1 shows the changes in gate-length and I_{off} according to *Intenational Technology Roadmap For Semiconductors* (ITRS) 2013. Current I_{off} contributes to static power.

Static CMOS is a logic circuit in which output is strongly driven because it is directly connected to either to V_{DD} or ground (GND). Fig. 2 shows the static CMOS logic which comprises of pull up network and pull down network. In case of pull-up, a connection is made from V_{DD} to *out* when *out* = 1. In case of pull-down, a connection is made from GND to *out* when *out* = 0. The number of gates are required are *2N* where N is the fan-in. In order to reduce the number of gates, logics like pseudo-NMOS, where NMOS is N-type metal-oxide semiconductor, pass transistor logic have been implemented [5]. But these circuits have large static power

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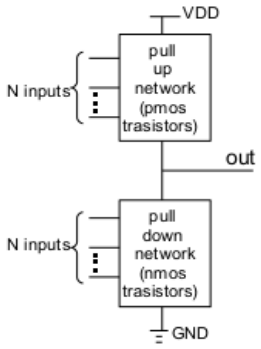

Fig. 2. A static CMOS logic.

dissipation. To reduce the static power dissipation, dynamic logic or clocked logic has been introduced. Dynamic logic uses only pull down network consisting of NMOS transistors to implement its logic. The block diagram of dynamic logic is shown in Fig. 3(a). It can be seen that the number of transistors are *N+2* which is less than the static CMOS. The main advantage of dynamic logic is that since the inputs are connected only to NMOS transistors, the input capacitance is less and thus dynamic logic operates faster than their static counterparts [6]. In dynamic logic, clock is distributed throughout and can lead to erroneous values in case of different timings of the clock in different parts of logic. If several stages of CMOS dynamic logic are cascaded using a single clock, a *race condition* can occur [7]. This can be solved with the help of domino logic which has an extra CMOS inverter at the output node as shown in Fig. 3(b).

Domino CMOS logic is used in variety of applications due to their high speed and low transistor count. But, due to leakage current and charge sharing, this logic has low noise immunity as compared to complementary CMOS logic [8]. Thus a PMOS (P-type Metal-Oxide Semiconductor) keeper is added in domino logic to compensate for the leakage current as shown in Fig. 4. But, the PMOS keeper has the disadvantage for degrading the performance of the device and contention currrent as explained in Section II.

Many logic techniques have been proposed earlier to improve the domino circuits in terms of performance, delay and area of the circuit.

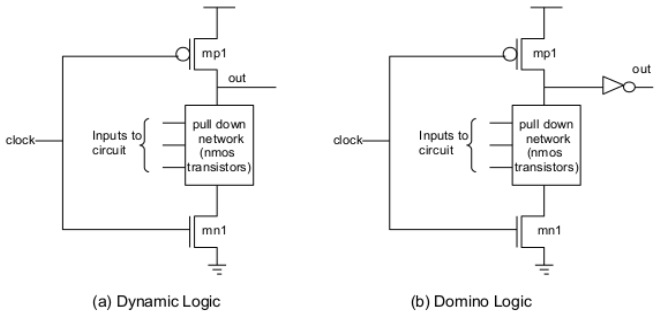

Fig. 3. Block diagrams of dynamic and domino logic.

For a given technology and gate topology, the product of power consumption and propagation delay is generally constant [5]. This product i.e. *power-delay-product* (PDP) is often used as a quality measure for a switching device. This paper also uses PDP as the metric to compare domino logic designs and to find the one that is fast and consume little energy.

A. Contribution

In this paper, a domino logic with modified keeper is proposed to improve the power dissipation and area of the circuit. The proposed design is compared with previous techniques of domino logic for six different values of aspect ratio of the keeper i.e W/L=1 to W/L=6. The design is improved as compared to existing designs for all the values of aspect ratio. The static power dissipation of the proposed design is reduced with respect to the previous techniques. For an 8-input OR gate and W/L=6, static power has reduced to 99.99% as compared to CDD and to 8.99% as compared to FDSTDL. The area of the circuit is also reduced making the design suitable for low power applications.

B. Organization of paper

Section II describes the functionality of domino logic and existing techniques of domino logic. Section III describes the proposed domino logic technique while Section IV discusses the results of the simulations performed on existing and proposed domino logic. Section V concludes the results of the proposed technique.

II. Literature Review

A. Domino Logic

Fig. 4 shows an 8-input OR-gate standard domino logic module. It consists of a clocked PMOS device *mp1*, pull down network consisting of only NMOS transistors, clocked NMOS device *mn1* and a static inverter producing non-inverting output, *out* [5]. A PMOS transistor *mp2* known as *keeper* is added to improve noise margins and to hold the value of output node *X* to *high* state during evaluation phase. The pull down network is built exactly as that in complementary CMOS. The domino module works in two phases – *precharge* and *evaluation*. Signal *clock* controls the mode of operation of domino as shown below:

$$clock = \begin{cases} 0, & \text{precharge phase} \\ 1, & \text{evaluation phase} \end{cases} \quad (1)$$

During *precharge* phase domino node *X* is charged to V_{DD} by PMOS transistor *mp1*. The clocked NMOS transistor *mn1* is *off* during this phase. Since the value of *out* becomes '0', keeper transistor *mp2* turns *on* which charges the value of node *X* to V_{DD}.

During *evaluation* phase, transistor *mp1* is *off* while *mn1* is in *on* state. If the input values *i1-i8* are such that pull down network conducts, then node *X* discharges to '0'. This will make the value of *out* to '1' and thus keeper turns *off*. If pull

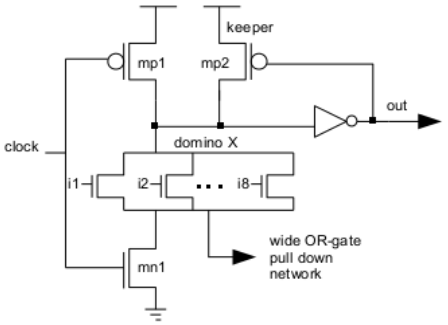

Fig. 4. Standard Domino Logic.

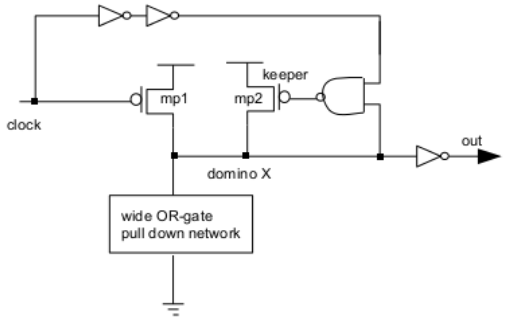

Fig. 5. Clock Delayed Domino Logic (CDD) [10].

down network is non-conducting then node *X* will retain the value of V_{DD} with the help of keeper transistor.

During the beginning of evaluation, keeper is *on* charging the node *X* to V_{DD}. If the input values makes pull down network in conducting state then node *X* discharges. This condition is called *contention* where one device tries to charge the node while other device tries to discharge it. In this case, there will be a direct path from V_{DD} to ground, thus, the circuit will suffer from large power dissipation. The size of the keeper is thus reduced to lower the contention current and to increase the evaluation speed [9]. But, lowering the size of the keeper will reduce the noise margin of the ciruit. Many techniques have been proposed in order to eliminate this speed-noise margin trade-off and thus to reduce the contention current.

B. Existing domino logic techniques

Wide fan-in domino logics are used in VLSI circuits and high performance microprocessors. A small PMOS keeper is required in domino logic to maintain the robustness of the circuit. If the number of inputs of domino logic increases, a large sized PMOS keeper is required. But, this in turn increases the contention current between PMOS keeper and NMOS pull down network, which degrades the performance of the circuit and increases the dynamic power loss. To eliminate this problem, a *clock delayed domino logic* (CDD) with keeper circuit is presented in [10]. Fig. 5 shows the concept of CDD, where *mp1* is the clock gated PMOS transistor and *mp2* is the keeper. Although this concept eliminates the contention current between PMOS keeper and NMOS pull down network [11], it has more power dissipation and area due to the additional nand gate.

In order to solve the trade-off between performance and noise-margin, a *high speed domino logic* (HSD) has been developed in [9] as shown in Fig. 6. In this technique, output signal *out* is connected to the keeper *mp2* via NMOS transistor *mn1* and PMOS transistor *mp3*. The gates of *mn1* and *mp3* are connected to delayed clock signal. This design reduces 60% of energy consumption as compared to standard domino logic [9].

A multi-V_{th} implementation of *high-speed domino logic* named here as MHSD was presented to reduce the power loss [9]. Its design is similar to that of HSD except that the source of keeper *mp2* is connected to signal $\overline{sleep}$ instead of

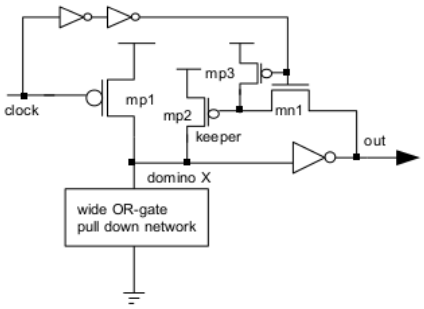

Fig. 6. High-Speed Domino Logic (HSD) [9].

V_{DD}. The signal *sleep* is '0' for active mode while it is '1' for standby mode of operation. Fig. 7 shows the circuit for MHSD logic where high V_{th} transistors are represented with a thick line in the channel region.

In order to further reduce the power dissipation, [11] have developed another domino logic named *clock delayed sleep mode* (CDSMD) domino logic. Fig. 8 shows the CDSMD logic which use sleep mode control circuitry and an odd number of inverters for the delayed clock. In CDSMD sleep signal is provided at the gate of transistors *mn2*, *mp4* and *mn5*.

The circuit shown in Fig. 9 is proposed in [12] for reducing the subthreshold leakage of domino logic circuits. This

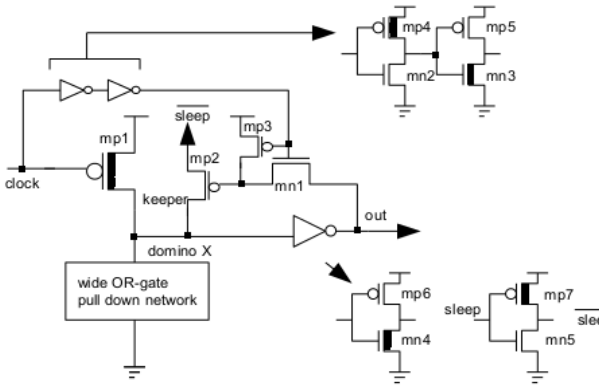

Fig. 7. Multi-V_{th} High Speed Domino Logic (MHSD) [9].

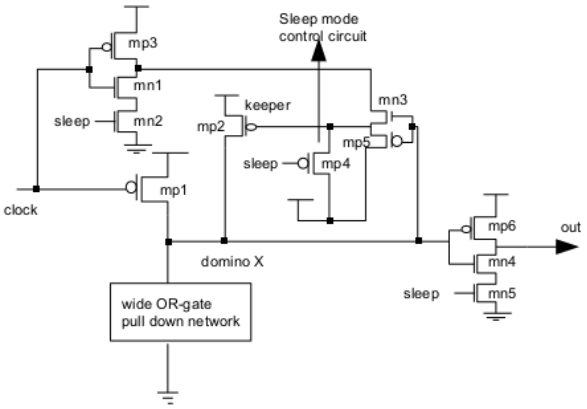

Fig. 8. Clock Delayed Sleep Mode Domino Logic (CDSMD) [11].

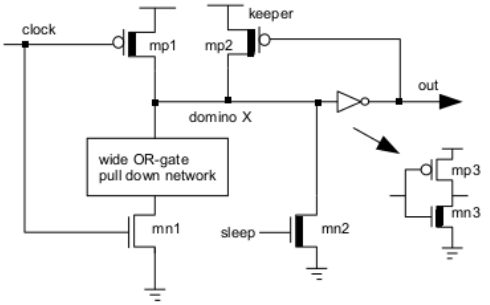

Fig. 9. Sleep Switch Dual-V_{th} Domino logic (SSDD) [12].

technique i.e *sleep switch dual domino* (SSDD), uses sleep switches and a dual threshold voltage in order to place an idle domino logic circuit into a low-leakage state. In Fig. 9 high V_{th} transistors *mp1*, *mp2*, *mn2* and *mn3* are represented with a thick line in the channel region. Another technique *PMOS only sleep switch dual-domino* (PSSDD) as shown in Fig. 10 uses PMOS only sleep switch transistors i.e. *mp4*, *mp5* and *mp7* to further reduce the leakage current in domino logic circuits [13]. In [14], work has been done to reduce the delay variation of the circuit which occur due to the feedback loop from output to input. Fig. 11 shows the circuit for *reduced delay variations domino logic* (RDVD). It uses a stack of PMOS transistors *mp2* and *mp3* as a modified keeper. Fig. 12 shows the configuration of *Foot Driven Stack Transistor Domino Logic* (FDSTDL). This circuit uses stack of NMOS transistors mn2 and mn3 to reduce the leakage current of the circuit.

In all the above designs, keeper is turned *off* during precharge phase in order to eliminate the contention current. During evaluation phase two condition exixts - pull down network is conducting or pull down network is non-conducting. If pull down network conducts, keeper is *off*. If pull down network is non-conducting, keeper is turned *on* and domino node *X* will maintain the value of V_{DD} with the help of keeper. Domino logic using CDD, HSD and CDSM have used single threshold voltage while Designs using MHSD,

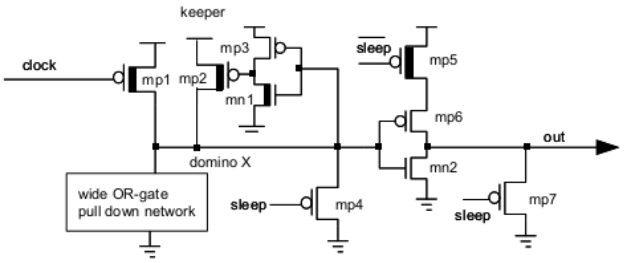

Fig. 10. PMOS Only Sleep Switch Dual-V_{th} Domino Logic (PSSDD) [13].

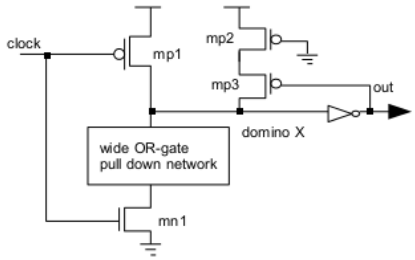

Fig. 11. Domino Logic with Reduced Delay Variations (RDVD) [14].

SSDD and PSSDD are dual threshold voltage designs. MHSD, SSDD, PSSDD and CDSM domino logic uses sleep mode control circuit which increases the area of the circuit and thus increases the power dissipation.

III. Proposed Domino Logic with Modified Keeper

Fig. 13 shows the the proposed domino logic with modified keeper circuit. The keeper consists of an NMOS transistor *mn2* which is connected in series to PMOS transistor *mp2*. The gate of *mn2* is connected to the clock while gate of *mp2* is connected to the output terminal i.e. *out*. During the precharge phase (*clock='0'*), *mp1* is *on*, which charges domino node *X*. Since transistor *mn2* is *off*, keeper is *off* at the beginning of evaluation. This will eliminate the contention current.

During evaluation phase (*clock='1'*), if pull down network conducts, node *X* will get discharged through *mn1*. In this case, since *out* is '1', *mp2* is *off* and thus keeper is *off*. If pull down network is non-conducting then, *out* is '0', *mp2* is *on* while since *clock* is '1' *mn2* is also *on*. Due to the presence of NMOS transistor in the keeper, node *X* will be retained to V_{DD}-V_{th}. But, since the domino node *X* is connected to the

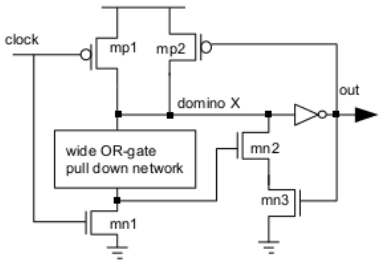

Fig. 12. Foot Driven Stack Transistor Domino Logic (FDSTDL) [15].

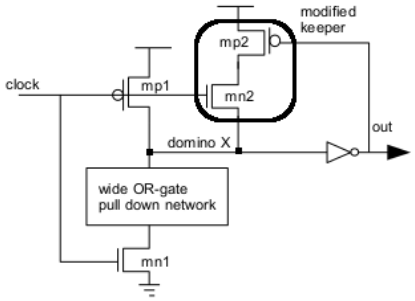

Fig. 13. Proposed domino logic.

input of the CMOS inverter, which is a noise robust device, the output of the domino logic will not be effected.

The proposed circuit is similar to standard domino logic except an addition of NMOS transistor in the modified keeper. This NMOS transitor is used in the proposed design to keep the keeper *off* at the beginning of evaluation and thus to eliminate the contention current and to reduce the power dissipation. The proposed design uses single threshold voltage without any sleep signal which reduces the area as compared to above mentioned designs.

Fig. 14 shows the output waveforms of the proposed domino logic. Here, v(vclk) is the voltage of input *clock*, v(v1) is input *i1*, v(vx) is the domino node *X* and v(vout) is the voltage of terminal *out*. The values of remaining inputs *i2-i8* is '0' and are not shown in the waveforms. The inputs (clock and i1) are taken such that to present the dynamic and static behavior of the proposed design. The rise time, fall time and delay of the input *i1* is 7.77×10^{-10} s, 7.77×10^{-10} s and 1×10^{-9} s respectively. The rise time, fall time and delay of output *out* is 4.35×10^{-9} s, 4.12×10^{-9} s and 3.65×10^{-9} s respectively.

IV. Results and Discussion

The Ngspice circuit simulator is used for simulating purpose. The 16nm PTM (predictive technology model) (level=54, version=4.0),is used to simulate the proposed technique as well as existing techniques of domino logic. The threshold voltages used during the simulation are mentioned in Table I. The supply voltage for all the designs is 0.9V. The width of PMOS transistor is 250nm while the width of NMOS transistors is 100nm. The width of the keeper transistor is kept at a lower value than that of width of NMOS transitors used in the design. The aspect ratio i.e. W/L of keeper is lowered from 6 to 1. The maximum width of keeper is 96nm while the minimum width is 16nm. The 8-input and 16-input OR gates has been chosen as the verifying circuits, because domino logic is usually used for wide fan-in OR gates. Every domino logic circuit is simulated to find dynamic power dissipation, static power dissipation, propagation delay and PDP for each value of W/L of keeper.

A. Results for 8-bit OR gate

Table II shows the dynamic power dissipation for various domino logic techniques. Fig. 15 shows the graphical representation of the dynamic power for the proposed and existing domino logic techniques. Table III shows the percentage comparison of dynamic power of proposed technique with respect to existing techniques. Positive percentage in Table III means that the existing technique has more dynamic power dissipation than the proposed technique. A negative percentage means that the existing technique have less dynamic power dissipation than the proposed technique. The dynamic power of the proposed technique is reduced significantly as compared to CDD, HSD and MHSD logics. There is a small increase in dynamic power in proposed technique as compared to CDSMD, SSDD, PSSDD and RDVD and FDSTDL logics. It is increased to a maximum of 8.00% as compared to CDSMD for W/L=6. It is also observed that dynamic power dissipation for a domino logic is almost constant for different W/L ratio of the keeper transistor.

TABLE I
Values of V_{TH} used during simulation

	NMOS	PMOS
Single V_{th} Designs	0.68V	-0.68V
Dual V_{th} Designs	0.68V, 0.48V	-0.68V, -0.43V

Table IV shows the average static power dissipation for various domino logic techniques. Fig. 16 shows the graphical representation of the static power for the proposed and existing domino logic techniques. Table V shows the percentage comparison of static power of proposed technique with respect to existing techniques. The static power dissipation of the proposed technique is reduced as compared to the existing domino logic techniques. For W/L=6, the static power is reduced to 99.99% as compared to CDD while to 8.99% as compared to FDSTDL. For W/L=1, the static power is reduced to 99.99% as compared to CDD while to -22.69% as compared to RDVD.

Table VI shows the propagation delay for various domino logic techniques. Fig. 17 shows the graphical representation of the delay for the proposed and existing domino logic techniques. Table VII shows the percentage comparison of delay of proposed technique with respect to existing techniques. For W/L=6, the delay of the proposed technique is reduced by 38.11% as compared to FDSTDL and it is increased to 23.38% as compared to SSDD. The delay of the proposed technique is increased as compared to the MHSD, SSDD and PSSDD techniques. This is because these techniques are dual threshold voltage techniques and thus have better performance than the proposed technique. The delay of proposed technique is reduced as compared to the rest of the techniques.

Table IX shows the PDP for various domino logic techniques. Fig. 18 shows the graphical representation of ppd for the proposed and existing domino logic techniques. Table X shows the percentage comparison of PDP of proposed technique with respect to existing techniques. It can be seen that PDP of the proposed technique is least as compared to the other techniques. For W/L=6, PDP is reduced to 99.99% as compared to CDD while it is reduced to 38.09% as compared to SSDD. PDP values of RDVD and FDSTDL are very close to the PDP values of proposed technique. Fig. 19 shows the

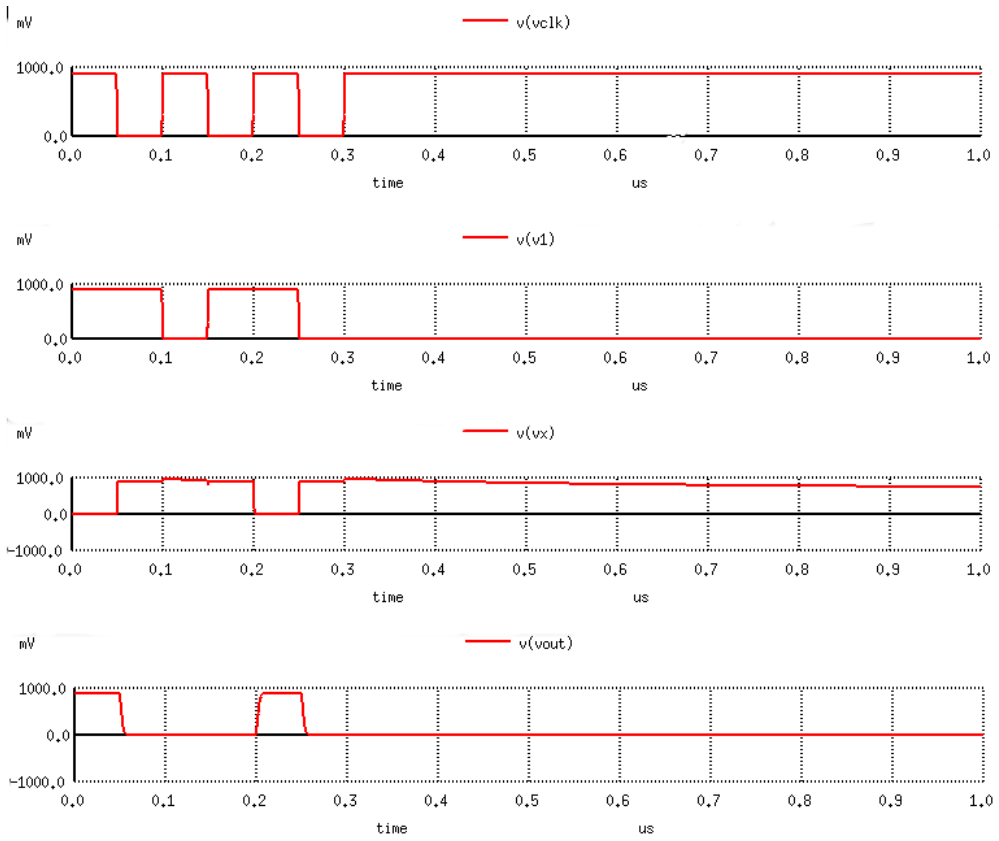

Fig. 14. Output waveforms of proposed domino logic for *i2-i8*='0'.

TABLE II
DYNAMIC POWER (WATTS) OF VARIOUS DOMINO LOGIC TECHNIQUES FOR 8-BIT OR GATE

Dyn. Power	CDD	HSD	MHSD	CDSMD	SSDD	PSSDD	RDVD	FDSTDL	Proposed
W/L=6	2.78×10^{-14}	1.34×10^{-15}	1.29×10^{-15}	8.25×10^{-16}	8.85×10^{-16}	9.09×10^{-16}	9.12×10^{-16}	5.15×10^{-16}	8.91×10^{-16}
W/L=5	2.78×10^{-14}	1.04×10^{-15}	1.23×10^{-15}	8.25×10^{-16}	8.76×10^{-16}	9.08×10^{-16}	8.86×10^{-16}	3.94×10^{-16}	8.81×10^{-16}
W/L=4	2.78×10^{-14}	9.50×10^{-16}	1.17×10^{-15}	8.25×10^{-16}	8.67×10^{-16}	9.06×10^{-16}	8.67×10^{-16}	3.61×10^{-16}	8.69×10^{-16}
W/L=3	2.78×10^{-14}	9.04×10^{-16}	1.10×10^{-15}	8.25×10^{-16}	8.58×10^{-16}	9.05×10^{-16}	8.52×10^{-16}	3.47×10^{-16}	8.57×10^{-16}
W/L=2	2.78×10^{-14}	8.70×10^{-16}	1.01×10^{-15}	8.25×10^{-16}	8.50×10^{-16}	9.04×10^{-16}	8.39×10^{-16}	3.37×10^{-16}	8.43×10^{-16}
W/L=1	2.78×10^{-14}	8.54×10^{-16}	9.67×10^{-16}	8.24×10^{-16}	8.45×10^{-16}	9.04×10^{-16}	8.27×10^{-16}	3.33×10^{-16}	8.31×10^{-16}

TABLE III
PERCENTAGE COMPARISON OF DYNAMIC POWER FOR 8-BIT OR GATE W.R.T. PROPOSED TECHNIQUE

Dynamic Power	CDD	HSD	MHSD	CDSMD	SSDD	PSSDD	RDVD	FDSTDL
W/L=6	96.79%	33.51%	30.93%	-8.00%	-0.68%	1.98%	2.30%	-73.01%
W/L=5	96.83%	15.29%	28.37%	-6.79%	-0.57%	2.97%	0.56%	-123.60%
W/L=4	96.87%	8.53%	25.73%	-5.33%	-0.23%	4.08%	-0.23%	-140.72%
W/L=3	96.92%	5.20%	22.09%	-3.88%	0.12%	5.30%	-0.59%	-146.97%
W/L=2	96.97%	3.10%	16.53%	-2.18%	0.82%	6.75%	-0.48%	-140.15%
W/L=1	97.01%	2.69%	14.06%	-0.85%	1.66%	8.08%	-0.48%	-149.55%

TABLE IV
STATIC POWER(WATTS) OF VARIOUS DOMINO LOGIC TECHNIQUES FOR 8-BIT OR GATE

Static Power	CDD	HSD	MHSD	CDSMD	SSDD	PSSDD	RDVD	FDSTDL	Proposed
W/L=6	8.55×10^{-6}	8.41×10^{-9}	5.33×10^{-9}	1.04×10^{-9}	1.44×10^{-9}	3.99×10^{-9}	1.19×10^{-9}	7.96×10^{-10}	7.24×10^{-10}
W/L=5	8.55×10^{-6}	6.89×10^{-9}	5.28×10^{-9}	1.05×10^{-9}	1.44×10^{-9}	3.99×10^{-9}	8.79×10^{-10}	7.81×10^{-10}	7.10×10^{-10}
W/L=4	8.55×10^{-6}	5.42×10^{-9}	5.27×10^{-9}	1.05×10^{-9}	1.44×10^{-9}	3.99×10^{-9}	7.96×10^{-10}	7.66×10^{-10}	6.97×10^{-10}
W/L=3	8.55×10^{-6}	4.05×10^{-9}	5.25×10^{-9}	1.06×10^{-9}	1.43×10^{-9}	3.99×10^{-9}	7.11×10^{-10}	7.52×10^{-10}	6.76×10^{-10}
W/L=2	8.55×10^{-6}	2.77×10^{-9}	5.29×10^{-9}	1.05×10^{-9}	1.43×10^{-9}	3.99×10^{-9}	6.27×10^{-10}	7.36×10^{-10}	6.75×10^{-10}
W/L=1	8.55×10^{-6}	2.15×10^{-9}	5.28×10^{-9}	1.06×10^{-9}	1.43×10^{-9}	3.98×10^{-9}	5.42×10^{-10}	7.22×10^{-10}	6.65×10^{-10}

TABLE V
PERCENTAGE COMPARISON OF STATIC POWER FOR 8-BIT OR GATE W.R.T. PROPOSED TECHNIQUE

Static Power	CDD	HSD	MHSD	CDSMD	SSDD	PSSDD	RDVD	FDSTDL
W/L=6	99.99%	91.39%	86.40%	30.48%	49.72%	81.85%	39.08%	8.99%
W/L=5	99.99%	89.70%	86.55%	32.12%	50.69%	82.18%	19.23%	9.09%
W/L=4	99.99%	87.14%	86.76%	33.65%	51.43%	82.51%	12.38%	8.95%
W/L=3	99.99%	83.31%	87.12%	35.92%	52.73%	83.04%	4.92%	10.05%
W/L=2	99.99%	75.63%	87.23%	35.90%	52.80%	83.06%	-7.74%	8.29%
W/L=1	99.99%	69.07%	87.41%	37.12%	53.50%	83.29%	-22.69%	7.89%

TABLE VI
DELAY(S) OF VARIOUS DOMINO LOGIC TECHNIQUES FOR 8-BIT OR GATE

Delay	CDD	HSD	MHSD	CDSMD	SSDD	PSSDD	RDVD	FDSTDL	Proposed
W/L=6	4.76×10^{-9}	7.41×10^{-9}	3.84×10^{-9}	5.80×10^{-9}	3.78×10^{-9}	4.27×10^{-9}	4.84×10^{-9}	7.53×10^{-9}	4.66×10^{-9}
W/L=5	4.49×10^{-9}	5.40×10^{-9}	3.81×10^{-9}	5.80×10^{-9}	3.75×10^{-9}	4.26×10^{-9}	4.68×10^{-9}	5.40×10^{-9}	4.59×10^{-9}
W/L=4	4.43×10^{-9}	4.84×10^{-9}	3.79×10^{-9}	5.79×10^{-9}	3.71×10^{-9}	4.25×10^{-9}	4.57×10^{-9}	4.83×10^{-9}	4.53×10^{-9}
W/L=3	4.39×10^{-9}	4.60×10^{-9}	3.75×10^{-9}	5.79×10^{-9}	3.68×10^{-9}	4.24×10^{-9}	4.48×10^{-9}	4.60×10^{-9}	4.46×10^{-9}
W/L=2	4.36×10^{-9}	4.45×10^{-9}	3.70×10^{-9}	5.79×10^{-9}	3.64×10^{-9}	4.23×10^{-9}	4.40×10^{-9}	4.45×10^{-9}	4.39×10^{-9}
W/L=1	4.34×10^{-9}	4.38×10^{-9}	3.67×10^{-9}	5.79×10^{-9}	3.62×10^{-9}	4.23×10^{-9}	4.33×10^{-9}	4.38×10^{-9}	4.33×10^{-9}

TABLE VII
PERCENTAGE COMPARISON OF DELAY FOR 8-BIT OR GATE W.R.T. PROPOSED TECHNIQUE

Delay	CDD	HSD	MHSD	CDSMD	SSDD	PSSDD	RDVD	FDSTDL
W/L=6	2.10%	37.11%	-21.35%	19.66%	-23.28%	-9.13%	3.72%	38.11%
W/L=5	-2.23%	15.00%	-20.47%	20.86%	-22.40%	-7.75%	1.92%	15.00%
W/L=4	-2.26%	6.40%	-19.53%	21.76%	-22.10%	-6.59%	0.88%	6.21%
W/L=3	-1.59%	3.04%	-18.93%	22.97%	-21.20%	-5.19%	0.45%	3.04%
W/L=2	-0.69%	1.35%	-18.65%	24.18%	-20.60%	-3.78%	0.23%	1.35%
W/L=1	0.23%	1.14%	-17.98%	25.22%	-19.61%	-2.36%	0.00%	1.14%

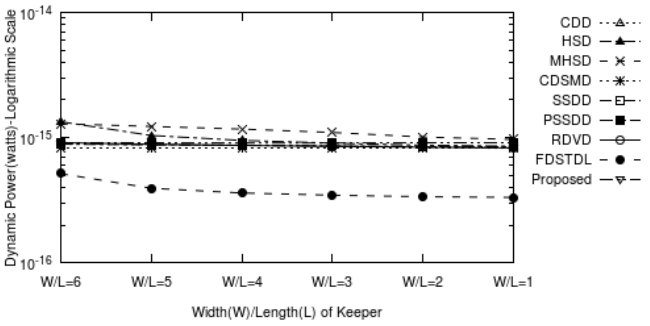

Fig. 15. Dynamic Power of various domino logic techniques for 8-bit OR gate.

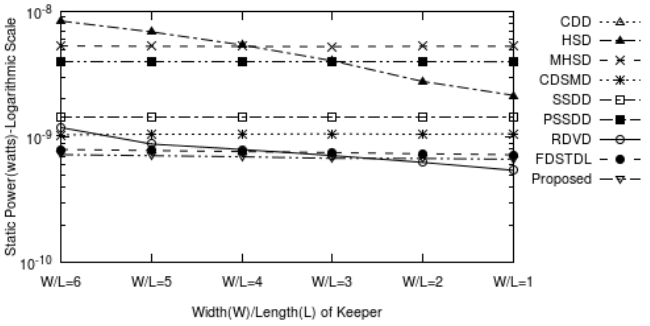

Fig. 16. Static Power of various domino logic techniques for 8-bit OR gate.

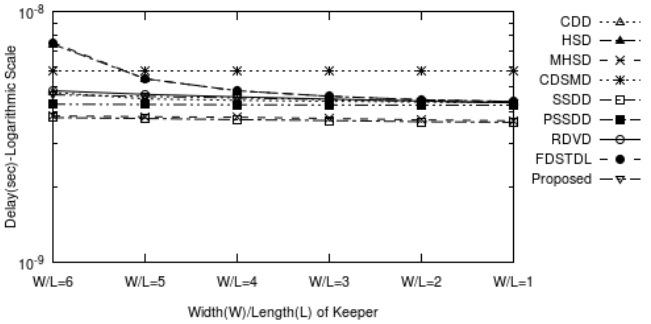

Fig. 17. Delay of various domino logic techniques for 8-bit OR gate.

comparison of PDP values RDVD, FDSTDL and proposed domino logic techniques.

Table XI shows the total number of transistors per domino logic module. The no. of transistors in the pull down network are not considered. There are six transistors in the proposed design which is minimum as compared to the existing techniques.

Rise time, fall time, delay, minimum output level (Min O/P) and maximum output level (Max O/P) of various domino logic techniques are shown in table VIII. The minimum input level is 0 V and maximum input level is 0.9 V. The parameter *delay* is the delay time from $t = 0ns$. All the parameters in Table VIII are for $W/L = 6$.

TABLE VIII
PARAMETERS OF OUTPUT WAVEFORM FOR VARIOUS DOMINO LOGIC CIRCUIT FOR 8-BIT OR GATE

Parameter	CDD	HSD	MHSD	CDSMD	SSDD	PSSDD	RDVD	FDSTDL	Proposed
Rise Time *(s)*	3.74×10^{-9}	4.21×10^{-9}	1.59×10^{-9}	3.74×10^{-9}	1.52×10^{-9}	6.03×10^{-9}	3.82×10^{-9}	4.04×10^{-9}	4.35×10^{-9}
Fall Time *(s)*	4.12×10^{-9}	4.12×10^{-9}	4.12×10^{-9}	9.52×10^{-9}	4.12×10^{-9}	2.11×10^{-9}	4.12×10^{-9}	4.13×10^{-9}	4.12×10^{-9}
Delay *(s)*	3.95×10^{-9}	3.99×10^{-9}	3.28×10^{-9}	3.65×10^{-9}	3.24×10^{-9}	3.23×10^{-9}	3.76×10^{-9}	4.01×10^{-9}	3.65×10^{-9}
Min O/P *(V)*	-1.25×10^{-4}	1.58×10^{-6}	1.32×10^{-4}	-9.55×10^{-5}	1.71×10^{-4}	7.49×10^{-5}	-1.43×10^{-4}	-1.77×10^{-4}	-8.77×10^{-5}
Max O/P *(V)*	0.9	0.9	0.9	0.9	0.89	0.9	0.9	0.9	0.9

TABLE IX
PDP(WATTS-S) OF VARIOUS DOMINO LOGIC TECHNIQUES FOR 8-BIT OR GATE

PDP	CDD	HSD	MHSD	CDSMD	SSDD	PSSDD	RDVD	FDSTDL	Proposed
W/L=6	4.07×10^{-14}	6.23×10^{-17}	2.04×10^{-17}	6.04×10^{-18}	5.44×10^{-18}	1.70×10^{-17}	5.75×10^{-18}	5.99×10^{-18}	3.37×10^{-18}
W/L=5	3.89×10^{-14}	3.72×10^{-17}	2.01×10^{-17}	6.07×10^{-18}	5.40×10^{-18}	1.70×10^{-17}	4.11×10^{-18}	4.22×10^{-18}	3.26×10^{-18}
W/L=4	3.79×10^{-14}	2.62×10^{-17}	1.99×10^{-17}	6.08×10^{-18}	5.32×10^{-18}	1.69×10^{-17}	3.63×10^{-18}	3.69×10^{-18}	3.16×10^{-18}
W/L=3	3.75×10^{-14}	1.86×10^{-17}	1.97×10^{-17}	6.11×10^{-18}	5.26×10^{-18}	1.69×10^{-17}	3.18×10^{-18}	3.46×10^{-18}	3.01×10^{-18}
W/L=2	3.73×10^{-14}	1.23×10^{-17}	1.95×10^{-17}	6.10×10^{-18}	5.20×10^{-18}	1.68×10^{-17}	2.75×10^{-18}	3.27×10^{-18}	2.96×10^{-18}
W/L=1	3.71×10^{-14}	9.42×10^{-18}	1.94×10^{-17}	6.12×10^{-18}	5.18×10^{-18}	1.68×10^{-17}	2.35×10^{-18}	3.16×10^{-18}	2.88×10^{-18}

TABLE X
PERCENTAGE COMPARISON OF PDP FOR 8-BIT OR GATE W.R.T. PROPOSED TECHNIQUE

PDP	CDD	HSD	MHSD	CDSMD	SSDD	PSSDD	RDVD	FDSTDL
W/L=6	99.99%	94.59%	83.52%	44.21%	38.09%	80.22%	41.42%	43.74%
W/L=5	99.99%	91.24%	83.79%	46.26%	39.63%	80.80%	20.75%	22.70%
W/L=4	99.99%	87.95%	84.16%	48.05%	40.64%	81.34%	13.08%	14.53%
W/L=3	99.99%	83.84%	84.71%	50.72%	42.80%	82.19%	5.50%	12.93%
W/L=2	99.99%	75.99%	84.86%	51.45%	43.13%	82.44%	-7.38%	9.62%
W/L=1	99.99%	69.52%	85.19%	53.13%	44.56%	82.95%	-22.29%	9.25%

TABLE XI
NO. OF TRANSISTORS PER DOMINO LOGIC MODULE FOR VARIOUS TECHNIQUES

CDD	HSD	MHSD	CDSMD	SSDD	PSSDD	RDVD	FDSTDL	Proposed
12	10	12	11	6	11	6	7	6

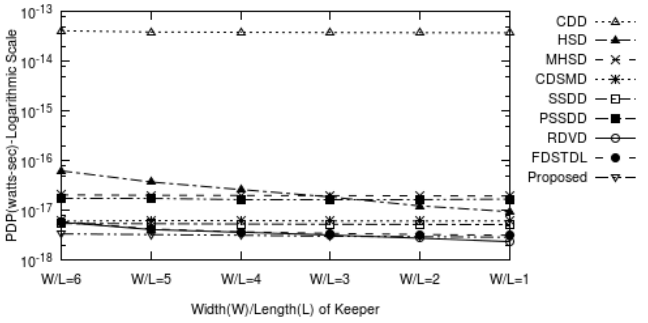

Fig. 18. Power-Delay-Product(PDP) of various domino logic techniques for 8-bit OR gate.

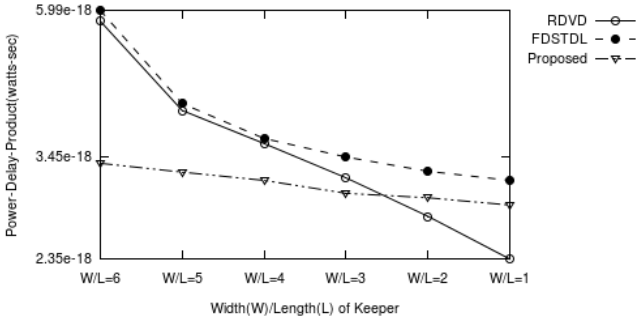

Fig. 19. Power-Delay-Product(PDP) of RDVD, FDSTDL and Proposed technique for 8-bit OR gate.

B. Results for 16 bit OR gate

Simulation have been carried out for existing and proposed techniques for 16 bit OR gate. Table XII shows the results for PDP values for 16-bit OR gate. Table XIII shows the comparsion of proposed techniques with respect to the existing techniques. For W/L=6, PDP is reduced to 99.99% as compared to CDD while it is reduced to 33.46% as compared to CDSMD.

C. Monte Carlo Simulation and Noise Analysis

An unavoidable process variations may occur during the integrated circuit fabrication, which may impact the static and dynamic characteristics of the circuit. In Monte Carlo analysis, various parameters are selected at random so as to check the performance of the circuit during variations. Various parameters varied for MOS transistors during *Monte Carlo* simulation are threshold voltage, mobility, oxide thickness,

TABLE XII
PDP(WATTS-S) OF VARIOUS DOMINO LOGIC TECHNIQUES FOR 16-BIT OR GATE

PDP	CDD	HSD	MHSD	CDSMD	SSDD	PSSDD	RDVD	FDSTDL	Proposed
W/L=6	4.15×10^{-14}	6.31×10^{-17}	3.03×10^{-17}	4.15×10^{-18}	5.49×10^{-18}	1.68×10^{-17}	4.81×10^{-18}	6.19×10^{-18}	2.76×10^{-18}
W/L=5	3.87×10^{-14}	3.74×10^{-17}	3.01×10^{-17}	4.17×10^{-18}	5.42×10^{-18}	1.67×10^{-17}	4.25×10^{-18}	4.38×10^{-18}	2.62×10^{-18}
W/L=4	3.82×10^{-14}	2.65×10^{-17}	3.01×10^{-17}	4.19×10^{-18}	5.38×10^{-18}	1.66×10^{-17}	3.76×10^{-18}	3.83×10^{-18}	2.49×10^{-18}
W/L=3	3.80×10^{-14}	1.89×10^{-17}	3.04×10^{-17}	4.21×10^{-18}	5.34×10^{-18}	1.66×10^{-17}	3.31×10^{-18}	3.58×10^{-18}	2.35×10^{-18}
W/L=2	3.76×10^{-14}	1.25×10^{-17}	3.10×10^{-17}	4.23×10^{-18}	5.28×10^{-18}	1.65×10^{-17}	2.88×10^{-18}	3.40×10^{-18}	2.23×10^{-18}
W/L=1	3.75×10^{-14}	9.61×10^{-18}	3.18×10^{-17}	4.25×10^{-18}	5.25×10^{-18}	1.65×10^{-17}	2.46×10^{-18}	3.29×10^{-18}	2.11×10^{-18}

TABLE XIII
PERCENTAGE COMPARISON OF PDP W.R.T. PROPOSED TECHNIQUE FOR 16-BIT OR GATE

PDP	CDD	HSD	MHSD	CDSMD	SSDD	PSSDD	RDVD	FDSTDL
W/L=6	99.99%	95.63%	90.88%	33.46%	49.69%	83.53%	42.61%	55.44%
W/L=5	99.99%	92.99%	91.30%	37.19%	51.70%	84.28%	38.38%	40.13%
W/L=4	99.99%	90.62%	91.74%	40.63%	53.73%	85.02%	33.80%	34.95%
W/L=3	99.99%	87.58%	92.27%	44.21%	55.98%	85.83%	28.92%	34.35%
W/L=2	99.99%	82.23%	92.81%	47.27%	57.77%	86.52%	22.55%	34.35%
W/L=1	99.99%	78.05%	93.36%	50.45%	59.82%	87.24%	14.28%	35.81%

TABLE XIV
RESULTS FOR MONTE CARLO ANALYSIS FOR PROPOSED CIRCUIT

Parameters	8-bit OR gate	16-bit OR gate
Mean (μ)(nW)	0.538	0.533
Standard Deviation (σ)(nW)	0.274	0.330
Variability (σ/μ)	0.510	0.561

TABLE XV
UNITY NOISE GAIN FOR VARIOUS DOMINO LOGIC TECHNIQUES FOR 16-BIT OR GATE

Technique	Unity Noise Gain (*Volts*)
CDD	0.705
HSD	0.761
MHSD	0.456
CDSMD	0.645
SSDD	0.349
PSSDD	0.340
RDVD	0.675
FDSTDL	0.755
Proposed	0.510

width and length. Generated random values for most of the parameters are nominal value plus variation drawn from Gaussian distribution with mean 0 and standard deviation 0.1 (relative to nominal), divided by sigma 3.

Fig. 20 shows the transient output for 50 runs of simulation for 8-bit OR gate and 16-bit OR gate. For the proposed domino logic the worst case is chosen with $0.9V_{DD}$ and 130°C and best case is chosen with $1.1V_{DD}$ at -30°C. Table XIV shows the results of monte carlo simulation for the proposed circuit. It can be seen that proposed circuit have lower variability and standard deviation. Thus the proposed circuit is reliable and robust.

The proposed design is suitable for low power applications with low power dissipation, low area and a little loss in performance. In order to perform the noise analysis, Unity Noise Gain (UNG) [15] is calculated. UNG is the amount of DC noise at all inputs that result in the same amount of noise at the output node [16]. Table XV shows the UNG of various domino logic techniques. A higher value of UNG shows better noise immunity.

Table XVI shows the comparison of the results (in percentages) showing the advantages and disadvantages of the proposed technique in relation to each of the existing ones. Here, the percentage shows the increase in performance of the proposed technique and is calulated using equation below:

$$Increase\ in\ Performance(\%) = \frac{PARAM_{existing} - PARAM_{\text{proposed}}}{PARAM_{proposed}} \cdot 100\% \quad (2)$$

where, $\text{PARAM}_{\text{existing}}$ is the parameter of the existing technique and $\text{PARAM}_{\text{proposed}}$ is the parameter of the proposed technique. In table XVI parameter *Pdyn* is the dynamic power, *Pstat* is the static power, *Delay* is the propagation delay, *Trise* is the rise time and *Tfall* is the fall time for 8-bit OR gate for W/L=6.

Below is the list which gives the summary of various techniques for domino logic.

- **CDD:** Low power dissipation. Large area due to nand gate.
- **HSD:** Reduces the tradeoff between performance and noise margin.
- **MHSD:** Dual threshold voltages are used in the design to reduce the leakage as well as delay.
- **CDSMD:** Sleep mode control circuitry is used thus, area is increased. High noise immunity.
- **SSDD:** Sleep switches as well as dual threshld voltages are used. More power, area and delay efficient. Low noise immunity.
- **PSSDD:** PMOS sleep transistors and a dual-threshold voltage CMOS technology are used to place an idle domino logic circuit into a low leakage state. Low noise immunity.
- **RDVD:** A modified keeper with a stack of two PMOS transistors are used. Less area with improved performance.
- **FDSTDL:** A stack of two NMOS transistors are used for reducing leakage. High noise immunity.

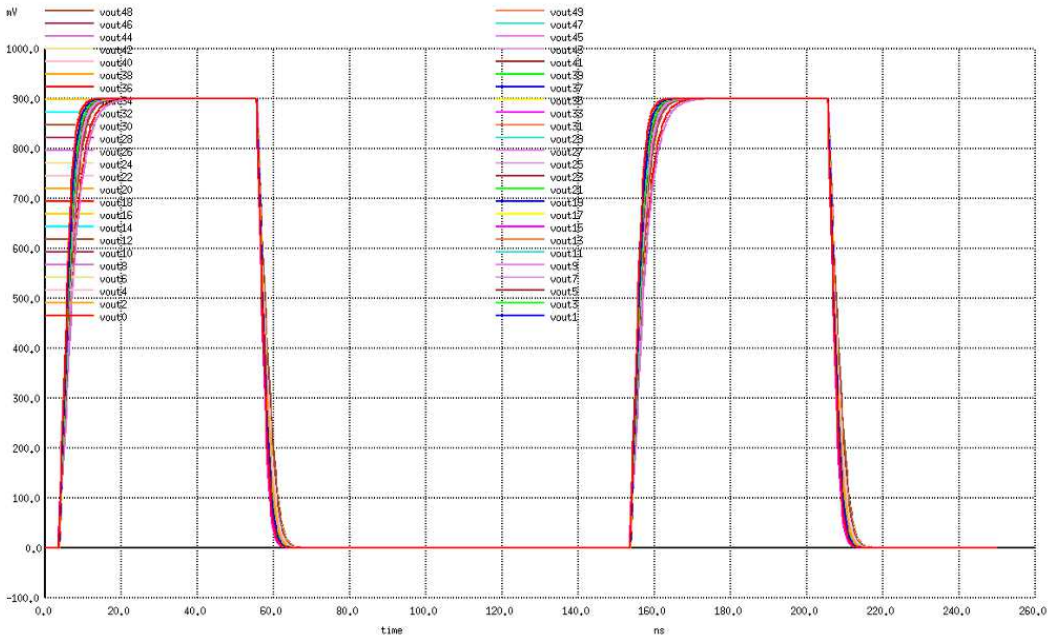

Fig. 20. Output of the Proposed Domino Logic during *Monte Carlo* Simulation.

TABLE XVI
COMPARISON OF PROPOSED TECHNIQUE WITH OTHER TECHNIQUES IN PERCENTAGES

Percentage(%)	Pdyn	Pstat	Delay	Trise	Tfall	PDP	Area	UNG
CDD	302009	118180117	215	-14	0	120770480	100	38
HSD	5039	106171	5901	-3	0	174810	67	49
MHSD	4478	63549	-1760	-63	0	50676	100	-10
CDSMD	741	4385	2446	-14	131	7924	83	26
SSDD	-67	9889	-1888	-65	0	6152	0	-31
PSSDD	202	45110	-837	38	-49	40556	83	33
RDVD	236	6415	386	-12	0	7069	0	32
FDSTDL	-4220	987	6159	-7	0	6931	17	48

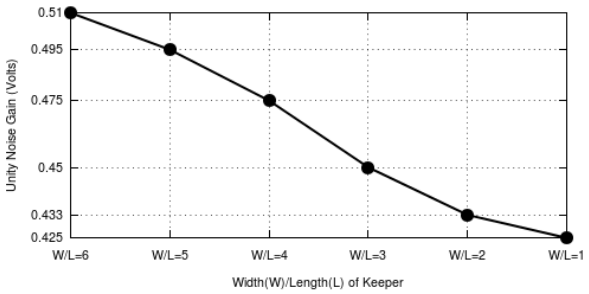

Fig. 21. Noise Analysis of Proposed technique for 16-bit OR gate.

- **Proposed:** A stack of one PMOS and one NMOS transistor is used as a modified keeper. Low leakage current.

V. CONCLUSION

The low power circuit has the feature of low power but with reduced speed. The proposed domino logic is best suited for low power applications without any area overhead. Proposed domino logic with modified keeper consists of NMOS and PMOS transistor in series. The gate of the NMOS transistor is connected to the clock while the gate of PMOS transistor is connected to the output terminal. This configuration will eliminate the contention current and reduces the power dissipation of the circuit. The PDP is improved as compared to *clock delayed domino logic* (CDD), *high speed domino logic* (HSD), *multi threshold high speed domino logic* (MHSD), *clock delayed sleep mode domino logic* (CDSMD), *sleep switch domino logic* (SSDD), *PMOS* only sleep switch domino logic (PSSDD), *reduced delay variations domino logic* (RDVD) and *Foot Driven Stack Transistor Domino Logic* (FDSTDL). Results have been calculated for different values of the W/L of keeper in order to check the behavior of the designs for lower widths of the keeper. For all values of W/L ranging for 1 to 6, the proposed design shows significant improvement in PDP. Thus, the proposed domino logic in an improved design with lesser area as compared to previous existing designs.

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