Single-Stage Operational Transconductance Amplifier Design in UTBSOI Technology Based on g_m/I_d Methodology

Rekib Uddin Ahmed, Eklare Akshay Vijaykumar, and Prabir Saha

***Abstract*—The downscaling of complementary metal-oxide-semiconductor (CMOS) technology is approaching its limits imposed by short-channel effects (SCE), thereby multi-gate MOSFETs have been proposed to extend the scalability. Ultra-thin-body silicon-on-insulator (UTBSOI) transistor is one of the dual-gated devices which offers better immunity towards SCEs. In this paper, two designs have been proposed for single-stage operational transconductance amplifiers (OTA) using the CMOS and UTBSOI. The CMOS based OTA (CMOS-OTA) has been designed where sizing (W/L) of the constituting MOSFETs have been evaluated through g_m/I_d methodology and the same OTA topology has been simulated using UTBSOI (UTBSOI-OTA) considering the same W/L. The DC simulation is carried out over the BSIM3v3 model to store the operating point parameters in the form of graphical models. The mathematical expressions for performance specifications have been applied over the graphical models to evaluate the required W/L. Individual comparisons between the two proposed designs have also been carried out for further applications. Based on simulation results at the schematic level, the UTBSOI-OTA has higher DC gain of $\approx$ 33.26% and lesser power consumption of $\approx$ 2.81% over the CMOS-OTA. Moreover, comparative analysis of performance parameters like DC gain and common-mode rejection ratio (CMRR), have been compared with the best-reported paper so far. In addition to this, the UTBSOI-OTA has been applied to practical integrator circuits for further verification.**

***Index Terms*—BSIM-IMG, g_m/I_d methodology, single-stage OTA, UTBSOI.**

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I. Introduction

THE demand for analog integrated circuit (IC) design will never diminish since the input signals fed to the transducers of any systems are analog in nature. CMOS analog design is a skill that develops upon experiences and intuition as there exists no specific set of rules which can be followed to design some analog blocks like OTA. In OTAs, the W/L of constituting MOSFETs moderately depend upon its performance parameters like DC gain, unity-gain bandwidth (UGB), slew rate (SR), input common-mode range (V_{iCMR}), common-mode rejection ratio (CMRR), and power. Conventional sizing procedure [1] calculated the W/L using the square-law model which was a tedious hand calculation design approach. On the other hand, more accurate and complex models [2] have been incorporated in the modern simulators. There exists a huge discrepancy between square-law and the models in simulators which prevents the possibility to meet the desired performance of the circuit. Though many advanced topologies for the single-stage OTA [3]–[10] have been reported so far but their sizing (W/L) procedure has not been discussed. In brief, although the circuit analysis for the OTAs is available, an elaborate description of the sizing procedure is lacking in the literature. The transconductance-to-drain current ratio (g_m/I_d) methodology [11] is an effective sizing procedure which can be applied to design any analog circuits.

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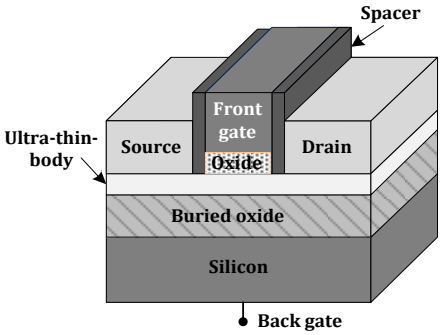

Fig. 1. Schematics showing 3-D view of the UTBSOI transistor.

Moreover, the process variation parameters of the non-classical MOSFETs have become a major cause in degrading the performance of such analog circuits. The short-channel effects (SCE) are becoming prone as the device dimension is scaled down to the nanoscale regime [12], [13]. Thus, a large abnormality is observed in the circuits produced by the present manufacturing process. Thereby, multi-gate MOSFETs like double-gate MOSFET, FinFET, and ultra-thin-body silicon-on-insulator (UTBSOI) have been proposed to overcome the limitations of SCEs [13]. The UTBSOI MOSFET as shown in Fig. 1 is a dual gated transistor has better scalability and superior controllability of gates over the shorter channel region. The superior gate controllability increases the transconductance, results in higher current drivability which in turn enhances the device speed. The UTBSOI also offers the flexibility of multiple threshold voltage control through its back-gate bias [14]. In low-power and high performance systems, the MOSFETs with different threshold voltages are

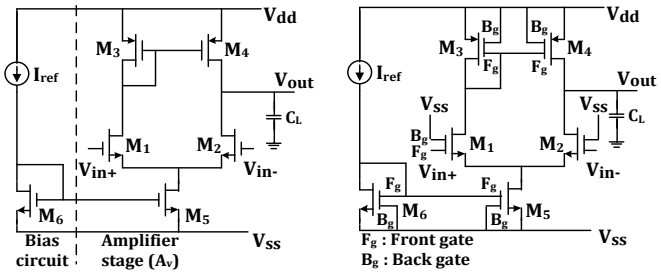

Fig. 2. Design of single-stage OTA using (a) CMOS, (b) UTBSOI.

TABLE I
DESIRED SINGLE-STAGE OTA SPECIFICATIONS

Specifications	Value
Technology	180 nm
Supply voltage	1.8 V
UGB	20 MHz
Open-loop DC gain (A_{vdc})	40 dB
PM	90°
CMRR	90 dB
SR	20 V/μs
$V_{iCM,min}$	-0.1 V
$V_{iCM,max}$	0.8 V
Reference current (I_{ref})	20 μA
Load capacitor	5 pF

required in the same circuit. The multiple threshold voltages in classical MOSFETs were achieved through using different channel doping concentrations. Whereas, in the UTBSOI, the same can be achieved by the use of back-gate bias instead of channel doping [15]. To utilize the benefits of UTBSOI, an accurate and fast computation model for device is required. BSIM-IMG [16] is the industry standard model for the UTB-SOI which have been validated with the hardware silicon based data from multiple technologies. However, the layout of UTBSOI is not possible till date due to the non-availability of the process-design kit in present simulators like Cadence-spectre [17].

In this paper, the g_m/I_d methodology has been adopted to design the single-stage OTA as shown in Fig. 2(a). This methodology considers intrinsic-gain (g_m/g_{ds}) versus g_m/I_d and normalized drain current (I_d/W) versus g_m/I_d graphs as the fundamental design tools to precisely calculate transistor's W/L [18], [19]. The relationship between g_m/g_{ds}, I_d/W and g_m/I_d are obtained by solving the mathematical expressions of performance parameters. The presented work in this paper improves the OTA designed in [19] with new set of specifications especially in terms of DC gain, PM, UGB, and CMRR. In addition to this, the UTBSOI- OTA [Fig. 2(b)] has been simulated at schematic level by utilizing the BSIM-IMG model. The design process has been performed in two phases: 1) The operating points parameters of both n- and p-type MOSFETs (BSIM3v3) obtained through DC simulation in spectre are stored in the form of a database, 2) This database corresponds to distinct parameters like drain current (I_d), g_m/g_{ds}, I_d/W with respect to g_m/I_d and have been used in MATLAB in the form of graphical models [Fig. 3$-$5] to calculate the W/L. The OTAs are simulated in Cadence-spectre using the generic process design kit (gpdk) 180-nm technology to extract the performance parameters. The use of UTBSOI in OTA has resulted improvements in terms of higher DC gain by $\approx 33.26\%$ and reduced power consumption by $\approx 2.81\%$ over that of CMOS-OTA.

II. PROPOSED DESIGN PROCEDURE

A single-stage five transistor OTA has got many uses in complex, analog, and mixed-signal systems. Despite its simplicity, the OTA has the frequency response in a desired limit. The transfer function of the OTA is expressed in terms of the operating point parameters as [21], [22]

$$A_v(s) = \frac{g_{m1,2}R_o}{1 + sC_LR_o} \tag{1}$$

where $g_{m1,2}$ is transconductance of the input pair ($M_{1,2}$), C_L is the load capacitance, and R_o =1/($g_{ds3} + g_{ds4}$) is the output resistance. The OTA has only one left-half plane (LHP) pole and no zero which ensures stability of the circuit. The PM is 90° due to a single pole.

The design procedure begins with information like power supply, technology, temperature, and the desired specifications. The required information, as given in Table I, have been taken from different sources [1], [19] and the g_m/I_d methodology has been employed to evaluate the sizing of such OTA. The DC simulation is performed on both n- and p-type MOSFETs where the drain-to-source voltage (V_{ds}) is set to ($V_{dd} - V_{ss}$)/3 and gate-to-source voltage (V_{gs}) sweep from -0.6 to 1 V is used. Since it is customary to use large channel width (W) in analog circuits, so the W is kept constant at 10 μm [19] and generally OTAs use long channel length (L) in order to achieve high DC gain [20], so parametric sweep of L = 180 nm to 2.58 μm has been used.

A. Design Procedure of Input Pair ($M_{1,2}$)

The transconductance of the input pair ($g_{m1,2}$) is calculated from the UGB and C_L specifications as follows [1]

$$UGB = \frac{g_{m1,2}}{2\pi C_L} \tag{2}$$

The OTA's internal capacitance is neglected as the load capacitance is much larger than the lumped parasitic capacitance [21]. Substituting the required values from Table I in (2) yields $g_{m1,2} \approx 628.31$ μS. Since, the desired SR is 20 V/μs, the current consumption of the OTA will be

$$I_{d5} = SR \times C_L \tag{3}$$

where I_{d5} (= 100 μA) is the current flowing through M_5. I_{d5} divides equally between M_1 and M_2 i.e. $I_{d1} = I_{d2}$ = 50 μA. The g_m/I_d of the input pair is calculated as

$$\left(\frac{g_m}{I_d}\right)_{1,2} \approx 13\ S/A \tag{4}$$

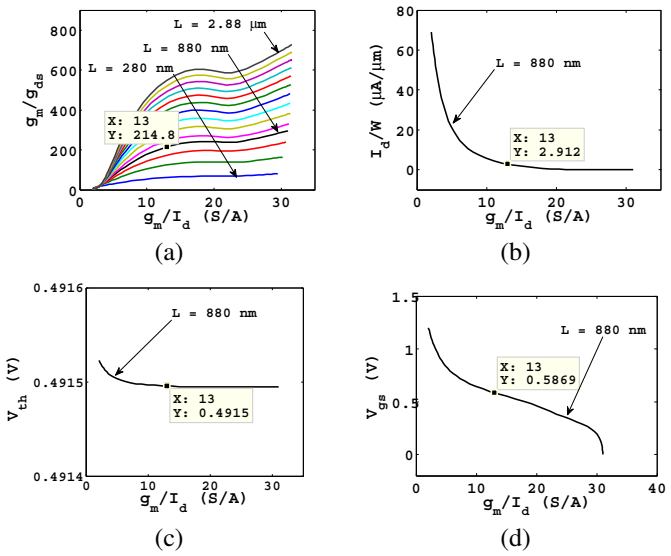

Fig. 3. Different parameters versus g_m/I_d of n-type input pair M_1, M_2 as a function of channel lengths (L = 280 nm: 200 nm: 2.88 μm) (a) intrinsic gain (g_m/g_{ds}), (b) normalized drain current (I_d/W), (c) V_{th}, (d) V_{gs}.

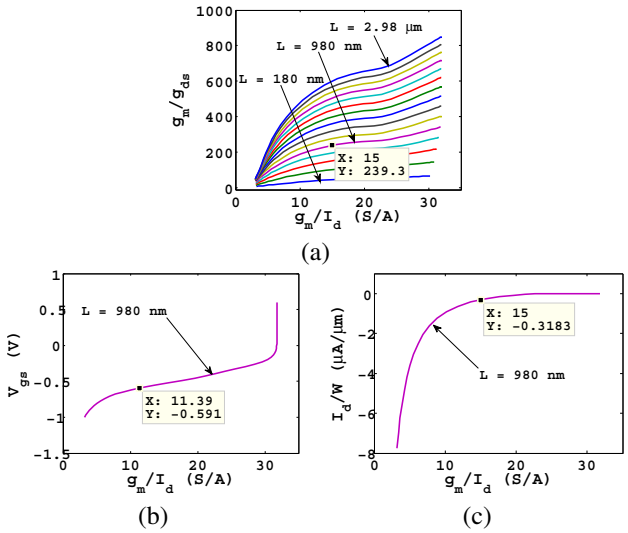

Fig. 4. Different parameters versus g_m/I_d of p-type current mirror load M_3, M_4 as a function of channel lengths (L = 180 nm: 200 nm: 2.98 μm) (a) intrinsic gain (g_m/g_{ds}), (b) V_{gs}, (c) normalized drain current (I_d/W).

The following relation gives the DC gain of the OTA [1]

$$A_{vdc} = \frac{g_{m1,2}}{g_{ds2} + g_{ds4}} \tag{5}$$

Substituting $g_{m1,2}$ and A_{vdc} in (5), the upper bound for the output conductance of M_2 and M_4 is obtained

$$g_{ds2} + g_{ds4} \leq 6.28\ \mu S \tag{6}$$

The inequality (6) splits equally between M_2 and M_4, which implies $g_{ds2} = g_{ds4} \leq 3.14\ \mu$S. The following equation gives the lower limit of intrinsic gain of input pair

$$\left(\frac{g_m}{g_{ds}}\right)_{1,2} \geq 200 \tag{7}$$

The graphical model in Fig. 3(a) shows the g_m/g_{ds} vs g_m/I_d plots for different channel lengths. At $(g_m/I_d)_{1,2}$ = 13 S/A, the plot for $L_{1,2}$ = 880 nm gives $(g_m/g_{ds})_{1,2} \approx 214.9$ which satisfies (7). For the selected $L_{1,2}$ (880 nm), the $W_{1,2}$ is calculated from the I_d/W vs g_m/I_d plot [Fig. 3(b)]. The current density $(I_d/W)_{1,2}$ = 2.91 μA/μm will give the required value of $W_{1,2}$ from the following relation

$$W_{1,2} = \frac{I_{d1,2}}{(I_d/W)_{1,2}} \approx 17.07\ \mu m \tag{8}$$

B. Design Procedure of Current Mirror Load ($M_{3,4}$)

The p-type MOSFETs, M_3 and M_4 are matched pair, so the output conductance of current mirror load are equal.

$$g_{ds3} = g_{ds4} \leq 3.14\ \mu S \tag{9}$$

In order to use the g_m/g_{ds} vs g_m/I_d graph, a large value of $(g_m/I_d)_{3,4}$ is required which is also essential from the power-efficient point of view [18], [20]. Selecting $(g_m/I_d)_{3,4}$ = 15 S/A results in $g_{m3,4}$ = 750 μ and thus the lower limit for intrinsic gain of current mirror load is obtained as

$$\left(\frac{g_m}{g_{ds}}\right)_{3,4} \geq 238.8 \tag{10}$$

From Fig. 4(a), the plot for $L_{3,4}$ = 980 nm satisfies the condition (10). The $(g_m/I_d)_{3,4}$ is also constrained by the maximum common-mode input ($V_{iCM,max}$) specification [1]. Applying KVL across the series of branch (M_3-M_1-M_5) of Fig. 2(a) will generate the constrained equation

$$V_{iCM,max} \leq V_{dd} + V_{gs3,4} + V_{th1,2} \tag{11}$$

$V_{th1,2}$ is extracted from the V_{th} vs g_m/I_d plot shown in Fig. 3(c), which is $\approx$ 0.4915 V. Substituting V_{dd}, $V_{th1,2}$, and $V_{iCM,max}$ in (11), the lower bound of $V_{gs3,4}$ is found as

$$V_{gs3,4} \geq -0.591\ V \tag{12}$$

By using V_{gs} vs g_m/I_d plot in Fig. 4(b), the valid range of $(g_m/I_d)_{3,4}$ due to the $V_{iCM,max}$ specification is found as

$$\left(\frac{g_m}{I_d}\right)_{3,4} \geq 11.39\ S/A \tag{13}$$

As a compromise, $(g_m/I_d)_{3,4}$ = 15 S/A is selected which satisfies (13) with adequate margin. $W_{3,4}$ is selected from the I_d/W vs g_m/I_d plot shown in Fig. 4(c), where $(I_d/W)_{3,4} \approx 0.3185$ μA/μm, thus $W_{3,4} \approx 156.96$ μm.

C. Design Procedure of Biased Current Sink ($M_{5,6}$)

The CMRR and minimum common-mode input ($V_{iCM,min}$) specifications decide the W/L of the biased current sink [1]. The CMRR is given by

$$CMRR(dB) = A_{vdc}(dB) - A_{vdc,CM}(dB) \tag{14}$$

where $A_{vdc,CM}$ is the common-mode DC gain. Substituting the required values in the following relation will give the limit of g_{ds5} [19].

$$A_{vdc,CM} = \frac{2g_{m1,2}g_{ds5}}{2g_{m1,2} + g_{ds5}} \cdot \frac{1}{2g_{m3,4}} \leq -50\ dB \tag{15}$$

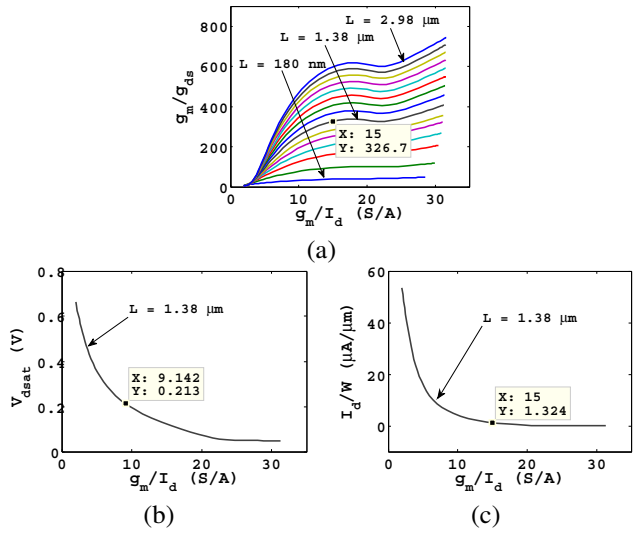

Fig. 5. Different parameters versus g_m/I_d of n-type biased current sink M_5 as a function of channel lengths ($L = 180$ nm: 200 nm: 2.98 μm) (a) intrinsic gain (g_m/g_{ds}), (b) V_{dsat}, (c) normalized drain current (I_d/W).

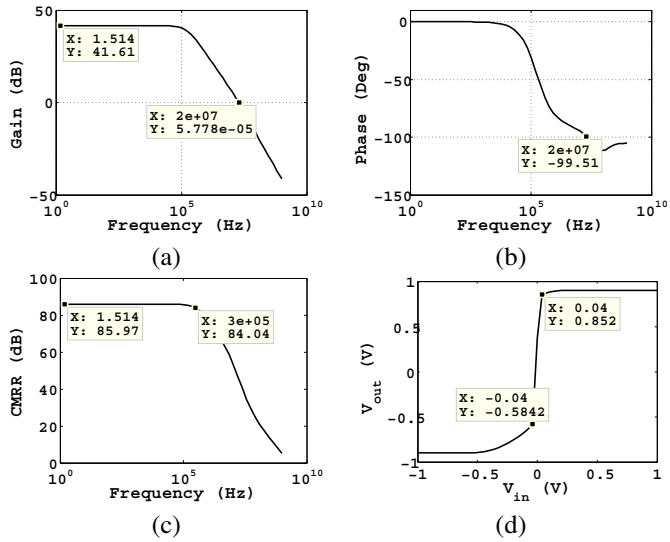

Fig. 6. Simulation results of the open-loop configuration of CMOS-OTA (a) DC gain, (b) phase, (c) CMRR, (d) output-voltage swing

$$\Rightarrow g_{ds5} \leq 4.76 \tag{16}$$

Similar to Section II-B, a large value for $(g_m/I_d)_5 = 15$ S/A is assumed which results in $g_{m5} = 1500$ μS and $g_m/g_{ds} \geq 315$. From Fig. 5(a), choosing $L_5 = 1.38$ μm satisfies this requirement. The $V_{iCM,min}$ that can be applied before driving the M_5 into saturation region is constrained by

$$V_{iCM,min} \geq V_{gs1,2} + V_{dsat5} + V_{ss} \tag{17}$$

Substituting the required values in (17), the constraint on V_{dsat5} is obtained as

$$V_{dsat5} \leq 0.213\ V \tag{18}$$

By using V_{dsat} vs g_m/I_d plot in Fig. 5(b), the valid range of $(g_m/I_d)_5$ due to the $V_{iCM,min}$ specification is obtained as

$$\left(\frac{g_m}{I_d}\right)_5 \geq 9.14\ S/A \tag{19}$$

As a compromise, $g_m/I_d = 15$ S/A is selected which satisfies (19) with a desired limit. The W_5 is selected from I_d/W vs g_m/I_d plot in Fig. 5(c), where $(I_d/W)_5 \approx 1.321$ μA/μm, thus, $W_5 \approx 75.66$ μm and $W_6 \approx 75.66/5 = 15.13$ μm.

TABLE II
SUMMARY OF TRANSISTOR'S SIZING AND CURRENT FLOWING THROUGH EACH OF THEM

Transistors	L (μm)	W (μm)	CMOS-OTA (μA)	UTBSOI-OTA (μA)
M_1, M_2	0.880	17.07	49.19, 49.20	47.77
M_3, M_4	0.980	156.96	49.19, 49.20	47.77
M_5, M_6	1.38	75.66, 15.13	98.40, 20.0	95.66, 19.88

III. Results and Discussions

Table II summarizes size of the MOSFETs and current flowing through each of them. The CMOS and UTBSOI-OTAs have been simulated under a supply voltage of 1.8 V ($V_{dd} = 0.9$ V, $V_{ss} = -0.9$ V) and characteristics of the open-loop and unity-gain configurations [1] are examined.

A. Simulation Results

Fig. 6 shows the simulated results obtained from the open-loop configuration of CMOS-OTA. Through the AC analysis simulation, the DC gain and UGB are $\approx$ 41.61 dB and 20.42 MHz, respectively as per the specified requirements. The other extracted parameters from AC analysis are PM and CMRR, simulated as 80.49° and 85.97 dB, respectively. The output-swing and power consumption have been extracted from DC analysis. The valid range of output-swing is ≈ -0.58 to 0.85 V as shown in Fig 6(d). In UTBSOI-OTA, the back gates of p- and n-type devices are connected to V_{dd} and V_{ss} respectively [Fig. 2(b)] so as to obtain static threshold voltage. The DC gain, UGB, PM, and CMRR of UTBSOI-OTA are simulated as 55.45 dB, 18.61 MHz, 74.6°, and 85.2 dB, respectively [Fig. 7]. The DC gain has seen to be improved in case of UTBSOI-OTA, whereas the UGB, PM, and CMRR are degraded within a tolerable limit. The valid output-swing is obtained as -0.73 to 0.86 V as shown in Fig. 7(d). The power consumption in case of CMOS-OTA is obtained as 0.213 mW and that of UTBSOI-OTA it is obtained as 0.207 mW.

The SR and V_{iCMR} have been extracted from the unity-gain (buffer) configuration. The valid buffer input range for the OTAs is obtained from the V_{out} vs V_{in} plots shown in Fig. 8(a) and (b). The SR of both the OTAs have been calculated from the unity-gain transient response as shown in Fig. 8(c) and (d). The SR is calculated using the relation: $(SR_+ + SR_-)/2$ which are obtained as 16.13 V/μs for CMOS and 15.74 V/μs for UTBSOI-OTAs. A summary of the

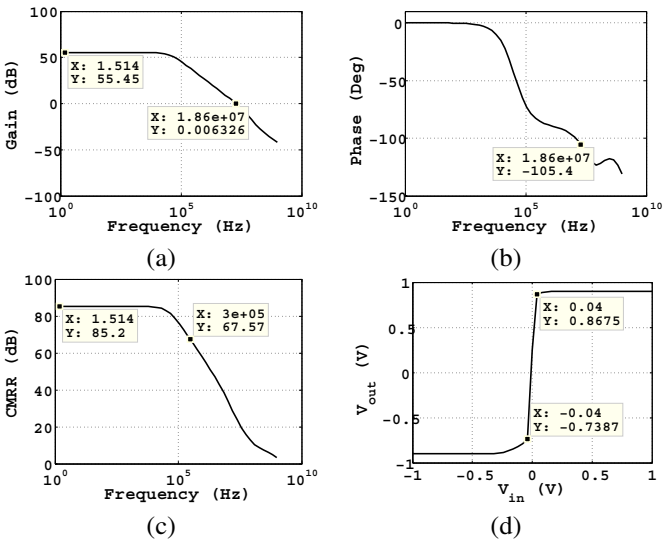

Fig. 7. Simulation results of the open-loop configuration of UTBSOI-OTA (a) DC gain, (b) phase, (c) CMRR, (d) output-voltage swing

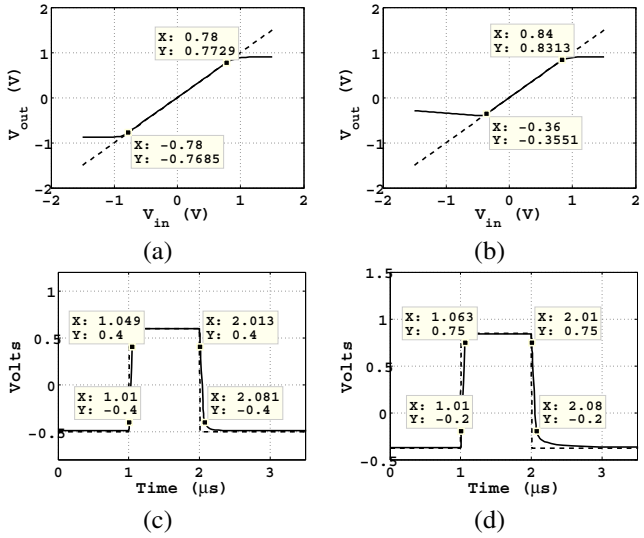

Fig. 8. Buffer input range of (a) CMOS-OTA, (b) UTBSOI-OTA and unity-gain transient response of (c) CMOS-OTA, (d) UTBSOI-OTA. (The V_{in} and V_{out} waveforms are represented by dashed and solid lines respectively).

simulation results of the OTAs is listed in Table III. Various performance parameters like DC gain, UGB, SR, PM, and power consumption are compared with prior reported works.

B. Layout Extraction of the CMOS-OTA

The layout design of the CMOS-OTA is shown in Fig. 9. In order to observe the impact of the extracted layout parasitics (resistance and capacitance) on the CMOS-OTA, the open-loop and unity-gain configurations of the OTA are simulated accordingly. Some deviations have been observed between the pre-layout [Table III], and post-layout simulation results, and the errors have been analyzed. The reason for the errors is related to inaccuracies associated with the parasitic components of the layout. Regarding the post layout simulation of the CMOS-OTA, the performance parameters like UGB, PM, DC gain, SR, CMRR, and power are degraded by 2.59%, 0.70%, 0.29%, 2.23%, 3.67%, and 2.34%, respectively as given in Table IV. The area of the CMOS-OTA extracted from the layout design is 2.78×10^{-3} mm^2.

TABLE III
PERFORMANCE COMPARISON WITH PRIOR REPORTED WORKS

Specifications	[6]	[7]	[19]	CMOS-OTA	UTBSOI-OTA
Technology (nm)	180	180	180	180	180
Supply voltage (V)	1.8	0.36	1.8	1.8	1.8
Load capacitor (pF)	200	-	5	5	5
UGB (MHz)	86.5	0.98	5	20.42	18.61
PM (°)	50	-	90	80.49	74.6
DC gain (dB)	72	18.4	33.5	41.61	55.45
Slew-rate (V/μs)	74.1	-	-	16.13	15.74
$V_{iCM,min}$ (V)	-	-	0.14	-0.179	-0.0015
$V_{iCM,max}$ (V)	-	-	1.12	0.778	0.997
CMRR (dB) @ DC	-	-	73.6	85.97	85.2
@ 300 KHz	-	45.3	-	84.04	67.57
Power (mW)	11.9	0.0154	-	0.213	0.207

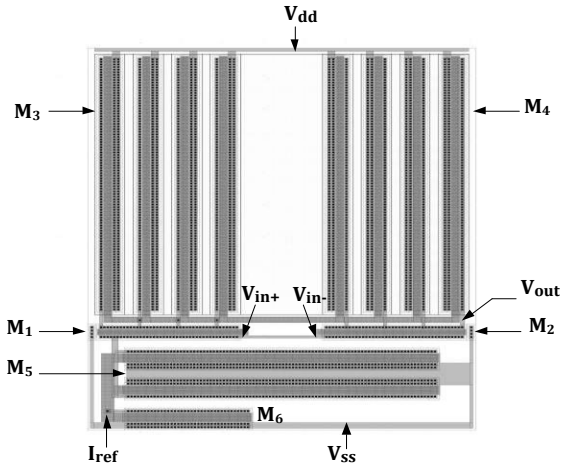

Fig. 9. Extracted layout view of the CMOS-OTA.

TABLE IV
SUMMARY OF POST-LAYOUT SIMULATED RESULTS OF CMOS-OTA

Specifications	Pre-layout results [Table III]	Post-layout results	Error (%)
UGB (MHz)	20.42	19.89	-2.59
PM (°)	80.49	79.92	-0.70
DC gain (dB)	41.61	41.49	-0.29
Slew-rate (V/μs)	16.13	15.77	-2.23
CMRR (dB) @ DC	85.97	82.81	-3.67
Power (mW)	0.213	0.218	2.34
Area (mm^2)	-	2.78×10^{-3}	-

The minus sign ($-$) shows the decrease in performance parameter values in post-layout simulation.

C. Applications of the UTBSOI-OTA

The UTBSOI-OTA has been tested by using it in the integrator circuits. Fig. 10(a) shows a basic integrator circuit (integrator 1) which is obtained from an inverting amplifier configuration by replacing the feedback resistor R_F with a capacitor C_F [23]. The unity-gain frequency of integrator 1 is $f_u = 1/(2\pi R_1 C_F)$, where, $R_1 = 15.9$ kΩ, $C_F = 0.01$ μF are chosen so as to generate $f_u = 1$ KHz. The circuit is tested

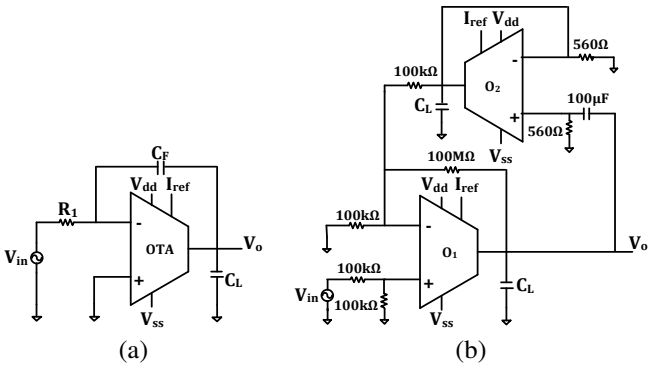

Fig. 10. The circuit diagram of (a) integrator 1, (b) integrator 2

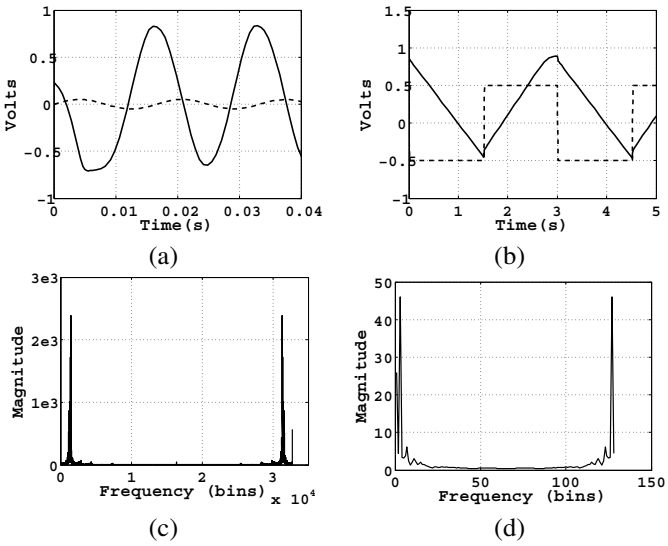

Fig. 11. Simulation results of UTBSOI-OTA based (a) integrator 1, (b) integrator 2. (c) 32K-point FFT for the output of integrator 1, (d) 128-point FFT for the output of integrator 2. (The V_{in} and V_{out} waveforms are represented by dashed and solid lines respectively).

by applying a sinusoidal input voltage of amplitude 24 mV at 60 Hz. Fig. 11(a) shows the output waveform obtained from the integrator 1. The validity of the OTA has been further verified by using it in a low-frequency integrator (integrator 2) [24] as shown in Fig. 10(b). A square wave voltage of amplitude $\pm$ 0.5 V at 330 mHz is applied which generates triangular wave output as shown in Fig. 11(b). Fig. 11(c) and (d) show the FFT obtained in MATLAB from the transient outputs of integrator 1 and integrator 2 respectively. From the FFT, the signal-to-noise ratio (SNR) and total-harmonic-distortion (THD) are calculated to acquire the signal-to-noise-and-distortion ratio (SNDR) as given in Table V. The relation used to calculate of the SNDR is [25]

$$SNDR = -10\ log\left[10^{-SNR/10} + 10^{-THD/10}\right] \qquad (20)$$

A good integration action is clearly seen from the above results which imply that the UTBSOI-OTA can be successfully used to design any analog circuits.

Addition to this, application of the UTBSOI-OTA has also been extended to active filters [26] in which the OTA is used for amplification and gain control. Fig. 12(a) shows

TABLE V
CALCULATED SNR, THD, AND SNDR OF THE INTEGRATOR CIRCUITS [FIG. 10]

Integrator circuits	SNR (dB)	THD (dB)	SNDR (dB)
Integrator 1	7.23	8.33	10.9
Integrator 2	10.34	−4.20	−10.02

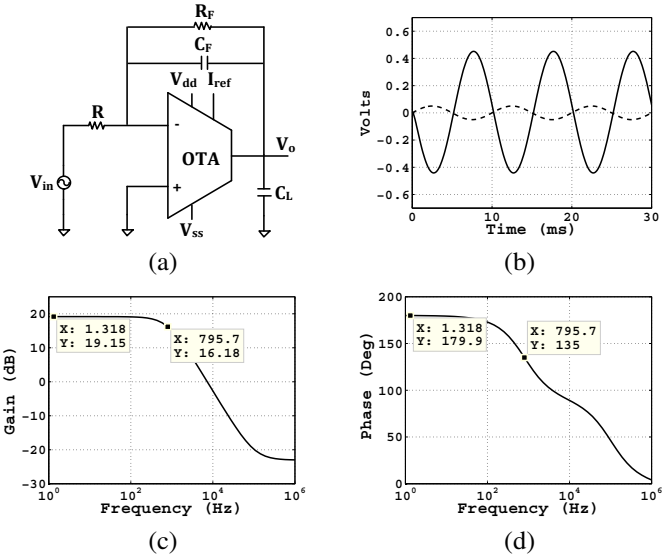

Fig. 12. Application of UTBSOI-OTA in (a) active low-pass filter, (b) transient response with sinusoidal input voltage of amplitude 50 mV at $f = 100$ Hz, (c) gain, (d) phase. (The V_{in} and V_{out} waveforms are represented by dashed and solid lines respectively).

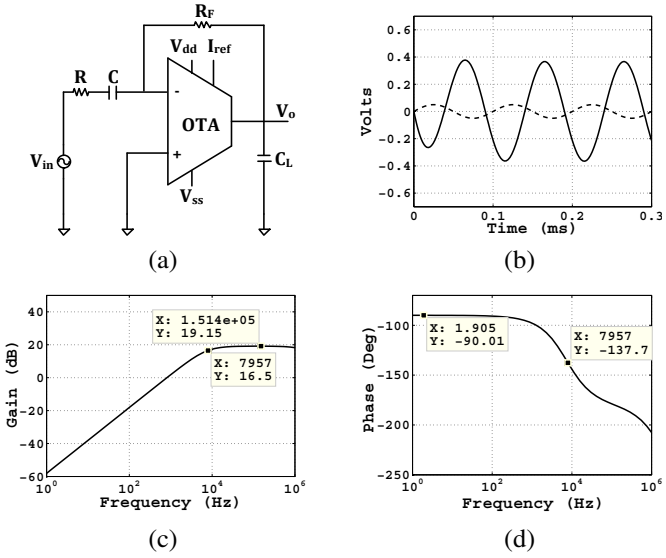

Fig. 13. Application of UTBSOI-OTA in (a) active high pass filter, (b) transient response with sinusoidal input voltage of amplitude 50 mV at $f = 10$ KHz, (c) gain, (d) phase. (The V_{in} and V_{out} waveforms are represented by dashed and solid lines respectively).

the first order low-pass filter having cut-off frequency ($f_c = 1/2\pi R_F C_F$) of 795.77 Hz with component values $R = 20$ kΩ, $C_F = 1$ nF, and $R_F = 200$ kΩ. The gain vs frequency plot in Fig. 12(c) clearly indicates the property of a low-pass filter with gain $\approx$ 19.15 dB which gets reduced by 3 dB

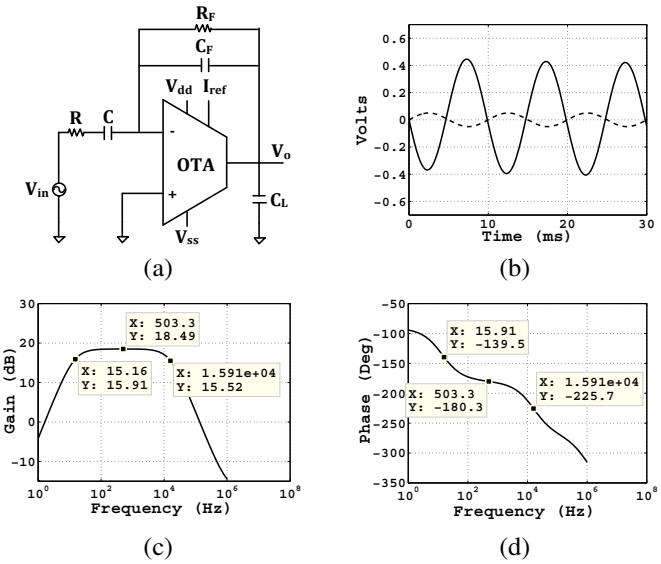

Fig. 14. Application of UTBSOI-OTA in (a) active band pass filter, (b) transient response with sinusoidal input voltage of amplitude 50 mV at $f = 100$ Hz, (c) gain, (d) phase. (The V_{in} and V_{out} waveforms are represented by dashed and solid lines respectively).

(=16.18 dB) at 795.77 Hz. Fig. 13(a) show the UTBSOI-OTA based first order high-pass filter in which component values $R = 20$ kΩ, $C = 1$ nF, and $R_F = 200$ kΩ are chosen to generate $f_c = 1/2\pi RC \equiv 7957.77$ Hz. Similarly, the second order band-pass filter in Fig. 14(a) is using the UTBSOI-OTA with component values $R = 10$ kΩ, $C = 1$ μF, $C_F = 100$ pF and $R_F = 100$ kΩ having the low ($f_L = 1/2\pi RC$) and high ($f_H = 1/2\pi R_F C_F$) cut-off frequencies of 15.91 Hz and 15.91 KHz. Simulation results of the active filters [Fig. 12−14] proves the applicability of UTBSOI-OTA in audio frequency applications.

IV. Conclusion

In this paper, single-stage OTA has been designed where the W/L of constituting MOSFETs have been evaluated mathematically and graphically through g_m/I_d methodology. Keeping the transistor's aspect ratio constant, the OTA has been designed through UTBSOI transistor. Simulation is performed in Cadence-spectre where BSIM3v3 and BSIM-IMG models have been utilized for MOSFET and UTBSOI respectively. Open-loop and unity-gain configurations are simulated accordingly to show a comparative analysis between the CMOS and UTBSOI based OTAs. In brief, the performance achieved by UTBSOI-OTA meets all the desired specifications within a desired limit. From the simulated results, it is observed that in sub-micron regime (180-nm), UTBSOI transistor can be successfully used to design the analog circuits. Advantage of the UTBSOI has been further clarified from the improvements of UTBSOI-OTA over the CMOS-OTA in terms of DC gain and power consumption by $\approx 33.26\%$ and 2.81%, respectively, through circuit simulation at the schematic level. Moreover, the UTBSOI-OTA has been verified by using it in integrator and active filter circuits which are able to show the desired output successfully. Based on the performance improvements obtained by applying the g_m/I_d methodology to UTBSOI at the schematic level simulation, it can be concluded that investing considerable effort into creating a process-design kit for the UTBSOI technology would be a very welcome step in enabling further improvements in analog and mixed-signal circuits results.

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References

[1] P.E. Allen and D.R. Holberg, *CMOS Analog Circuit Design*, 3rd ed. London, UK.: Oxford Univ. Press, 2014.

[2] W. Liu and C. Hu, "BSIM3v3 MOSFET model," *Int. J. of High Speed Electron. Syst.*, vol. 9, no. 3, pp. 671−701, Sep. 1998.

[3] J.R-. Angulo, B. Calvo, R.G. Carvajal, and A.L-. Martin, "Low-voltage gm-enhanced CMOS differential pairs using positive feedback," in *Proc. IEEE Int. Symp. Circuits Syst.*, Paris, 2010, pp. 773−776.

[4] M.R.V. Bernal, S. Celma, N. Medrano, and B. Calvo, "An ultralow-power low-voltage class-AB fully differential OpAmp for long-life autonomous portable equipment," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 59, no. 10, pp. 643˘647, Oct. 2012.

[5] M. Akbari, "Single-stage fully recycling folded cascode OTA for switched-capacitor circuits," *Electron. Lett.*, vol. 51, no. 13, pp. 977−979, Jun. 2015.

[6] S. Sutula, M. Dei, L. Terés, and F.S-.Graells, "Variable-mirror amplifier: a new family of process-independent class-AB single-stage OTAs for low-power SC circuits," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 63, no. 8, pp. 1101−1110, Aug. 2016.

[7] L. Severo and V. Noije, "0.36 V PGA combining single-stage OTA and input negative transconductor for low energy RF receivers," *Electron. Lett.*, vol. 54, no. 5, pp. 977−979, Mar. 2018.

[8] A.J.L-.Martin *et al*., "Enhanced single-stage folded cascode OTA suitable for large capacitive loads," *IEEE Trans. Circuits Syst. II: Express Briefs*, vol. 65, no. 4, pp. 441−445, Apr. 2018.

[9] R. Póvoa *et al*., "Single-stage OTA biased by voltage combiners with enhanced performance using current starving," *IEEE Trans. Circuits Syst. II: Express Briefs*, vol. 65, no. 11, pp. 1599−1603, Nov. 2018.

[10] Q. Zhang, Y. Wang, X. Zhao, and L. Dong, "Single-stage multipath class-AB bulk driven OTA with enhanced power efficiency," *AEU-Int. J. Electron. Commun.*, vol. 107, pp. 39−48, Jul. 2019.

[11] F. Silveira, D. Flandre and P.G.A. Jespers, "A gm/ID based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA," *IEEE J. Solid-State Circuits*, vol. 31, no. 9, pp. 1314−1319, Sep. 1996.

[12] I. Ferain, C.A. Colinge, and J.-P. Colinge, "Multigate transistors as the future of classical metal-oxide-semiconductor field-effect transistors," *Nature*, vol. 479, pp. 310−316, Nov. 2011.

[13] N. Paydavosi *et al*., "BSIM-SPICE models enable FinFET and UTB IC designs," *IEEE Access*, vol. 1, pp. 201−215, May 2013.

[14] Q. Liu *et al.*, "Ultra-thin-body and BOX (UTBB) fully depleted (FD) device integration for 22 nm," in *Proc. Symp. VLSI Technol.*, Honolulu, 2010, pp. 61−62.

[15] S. Khanderwal *et al*., "BSIM-IMG: A compact model for ultrathin-body SOI MOSFETs with back-gate control," *IEEE Trans. Electron Devices*, vol. 59, no. 8, pp. 2019−2026, Aug. 2012.

[16] BSIM-IMG Model. (2017, Aug. 10). [Online]. Available: http://bsim.berkeley.edu/models/bsimimg/

[17] C. Hu *et al*., *Industry Standard FDSOI Compact Model BSIM-IMG for IC Design*, 1st ed. Woodhead Pub., 2019.

[18] T. Konishi, K. Inaju, J.G. Lee, M. Natsui, S. Masui, and B. Murmann, "Design optimization of high-speed and low-power operational transconductance amplifier using gm/ID lookup table methodology," *IEICE Trans. Electron.*, vol. E94-C, no. 3, pp. 334−345, Mar. 2011.

[19] M.N. Sabri, H. Omran, and M. Dessouky, "Systematic design and optimization of operational transconductance amplifier using gm/ID design methodology," *Microelctronics J.*, vol. 75, pp. 87−96, May 2018.

[20] V. Subramanian *et al*., "Impact of fin width on digital and analog performances of n-FinFETs," *Solid-State Electron*, vol. 51, no. 4, pp. 551−559, Apr. 2007.

[21] K.N. Leung and P.K.T. Mok, "Analysis of multistage amplifier-frequency compensation," *IEEE Trans. Circuits Syst. I: Fundam. Theory Appl.*, vol. 48, no. 9, pp. 1041−1056, Sep. 2001.

[22] M. Yang and G.W. Roberts, "Synthesis of high gain operational transconductance amplifiers for closed-loop operation using a generalized controller-based compensation method," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 63, no. 11, pp. 1794−1806, Nov. 2016.

[23] R.A. Gayakwad, *Op-amps and Linear Integrated Circuits*, 4th ed. New Delhi, India: PHI., 2010.

[24] M.A. Al-Alaoui, "Low-frequency differentiators and integrators for biomedical and seismic signals," *IEEE Trans. Circuits Syst. I: Fundam. Theory Appl.*, vol. 48, no. 8, pp. 1006−1011, Aug. 2001.

[25] W. Kester, "Understand SINAD, ENOB, SNR, THD, THD + N, and SFDR so you don't get lost in the noise floor," Analog Devices, Norwood, MA, USA, Tech. Rep. MT-003, 2009.

[26] S. Franco, *Design with Operational Amplifiers and Analog Integrated Circuits*, 3rd ed. New York: McGraw-Hill, 2013.