

A Novel Dual Output Schmitt Trigger Using Second Generation Current Controlled Conveyor

Avireni Srinivasulu, Syed Zahiruddin, and Musala Sarada

Abstract—Schmitt trigger is designed using the single second generation Current Controlled Conveyor. The proposed configuration utilizes single CCCII and only two externally connected resistors and is able to produce dual output square wave signal. The topology has the benefit of having a simple circuit, offering a large bandwidth and improved slew rate. PSPICE simulator using OrCad 16.3 version, 0.35 μm CMOS technology is used to verify the design, hysteresis is determined and compared with the existing methods available in the literature. The proposed configuration is tested using the experimental setup involving CFOA (AD844AN) and OTA (LM13700). The results have been found satisfactory in both simulation and experimental aspect. Montecarlo analysis and worstcase analysis are determined to prove the circuit efficiency in terms of critical parameters such as resistance with a tolerance of 5%. The hysteresis is also determined, that can reduce the effect of noise, able to produce exact square wave at the output. Schmitt trigger circuits find the applications in the field of Bio medical applications, analog signal processing, communication systems, waveform generators, pulse width modulators, multivibrators, flip-flops and in many other amplifier circuits. The basic application of Schmitt trigger is a square wave generator. The proposed topology is the best suited for monolithic IC fabrication.

Index Terms— CCCII, CFOA, current conveyor, hysteresis, OTA, Schmitt trigger.

Original Research Paper
DOI: 10.7251/ELS2024047S

I. INTRODUCTION

SCHMITT and Square waveform generators with controllable frequency are widely used circuits in the fields of bio medical applications, instrumentation and measurement

Manuscript received 8 January 2020. Received in revised form 22 March 2020 and 28 April 2020. Accepted for publication 13 May 2020.

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[1]-[2]. These serve as interfaces for signal processing, as they offer better electromagnetic interference immunity, lower sensitivity, and has simpler structures compared to harmonic oscillators based on a linear positive feedback structure. Due to these advantages, many relaxation oscillators have been published recently [3]-[11]. The configuration of relaxation oscillator habitually consists of a Schmitt trigger and an integrator in a closed loop. Designers employed various active elements to realize these blocks [5], [8], [9], [12], [13]. Initially operational amplifiers were used, followed by operational transconductance amplifiers (OTAs), second generation current conveyors (CCIIs), differential difference current conveyors (DDCCs), current differencing transconductance amplifiers (CDTAs), differential voltage current conveyor (DVCC), current feedback operational amplifiers (CFOAs) etc., were used to realize waveform generators [12]-[30].

The manuscript presents a novel dual output Schmitt trigger with single current controlled conveyor, with only two resistances and without any capacitance. This makes the circuit attractive for integrated circuit implementation. High-impedance voltage input is used to get accurate, linear, and wideband control of oscillation frequency. High impedance is realized due to the impact of intrinsic resistance that is controlled by the dc bias current. The topology has CCCII as active element which offers the advantages of wider bandwidth, high slew rate, better accuracy and high dynamic range with low supply voltage as compared to the conventional operational amplifiers and other configurations available in the literature.

II. CURRENT CONVEYOR

A. Current Mode Circuits

For the past few decades, analog designers have trusted current-mode circuits as an essential part of analog circuits. Smith and Sedra had invented the first generation current conveyor (CCI), employing bipolar junction transistors [1], [2], [7]. It has been preferred over the conventional operational amplifiers that were used to realize many applications, but CCI has the limitation of low input impedance. The modified CCI, called as second generation current conveyor (CCII) was introduced by the same duo in 1970. It has high input impedance and preferred in realizing many applications such as oscillators, filters, instrumentation amplifiers and many more. Instead, CCII faces the limitation

of lack of electronic tunability. CCCII, a series of CCII, is a three terminal device with two input ports X and Y and output port Z and has the intrinsic resistance at input port X which is current controlled. Thus, it has introduced the concept of Current Controlled Conveyor (CCCII) [4], [6], [9].

B. Second Generation Current Controlled Conveyor (CCCII)

Originally, CCCII is the current mode active structural element and possess mixed translinear loop that has considerable amount of intrinsic resistance (R_B) at the input node X . It is varied by tuning the external bias current (I_B).

The ideal characteristics of CCCII, involving the intrinsic resistance (R_B) is portrayed in the below matrix.

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & R_B & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (1)$$

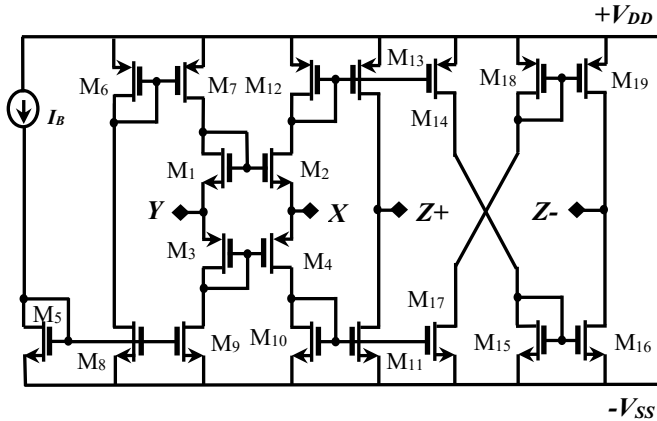


Fig. 1. Internal composition of CCCII±

CCCII is a three port device, two input terminals X and Y along with an output terminal Z . The device is characterized by $I_Y = 0$, $V_X = V_Y + R_B I_X$ and $I_Z = \pm I_X$, shown in the matrix form in (1). From (1), if the direction of current at input port X and output port Z are same, it is called a positive current conveyor (CCCII+). If the direction of current is opposite to each other then it is a negative current conveyor (CCCII-) [1], [2]. The device has an infinite input impedance at terminal Y and Z , whereas, the input terminal X has intrinsic resistance R_B which is altered by the external bias current I_B , given as:

$$R_B = \frac{1}{g_{m2} + g_{m4}} \quad (2)$$

where g_{m_i} is the transconductance of the MOS transistor, presuming that both the transistors are matched, $g_{m2} = g_{m4}$, then:

$$R_B = \frac{1}{\sqrt{8\mu C_{OX} \left(\frac{W}{L}\right)} I_B} \quad (3)$$

where μ signifies the surface mobility, C_{OX} denote the oxide capacitance, W and L are the channel width and length of the MOS transistors (M_2 and M_4) respectively. The schematic of CCCII is realized with MOS transistors, and shown in Fig. 2. The circuit is composed of translinear loop implying that transistors M_1 to M_4 , DC biased by using the current mirrors M_6 - M_7 and M_8 - M_9 . The input current I_X is duplicated to produce I_Z using the current mirrors M_{10} - M_{11} and M_{12} - M_{13} . The current is reflected using additional current mirrors M_{14} - M_{19} .

Several applications are presented by applying bias current to the CCCII [20]-[34]. Fig. 1 shows the symbol of CCCII.

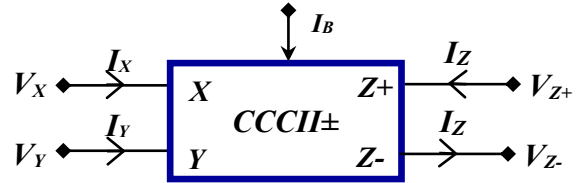


Fig. 2. Symbol of CCCII

III. SCHMITT TRIGGER USING CCCII

Fig. 3 shows the proposed Schmitt trigger and waveform generator involving CCCII as an active device.

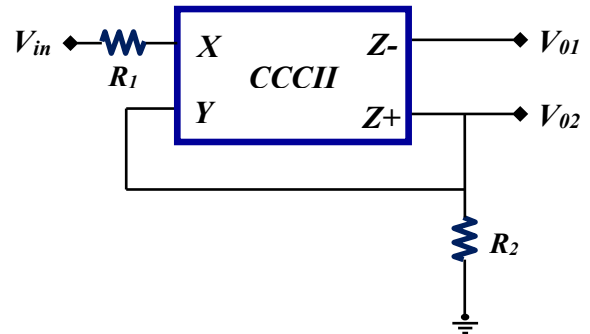


Fig. 3. Proposed dual output Schmitt trigger using CCCII

The configuration shown in Fig. 3 basically act as a comparator with positive feedback. The loop gain βV_{02} , (where $\beta = R_2 / [R_2 + R_B]$ is the feedback gain) is fed as input to the port Y . The input voltage, sinusoidal signal is applied to input port X . The input voltage V_{in} triggers the output V_{02} whenever it exceeds certain voltage levels called upper threshold voltage (V_{UT}) and lower threshold voltage (V_{LT}). As long as V_{in} is less than V_{UT} the output remains at $+V_{sat}$ at output V_{02} . When V_{in} just exceeds V_{UT} , the output regeneratively switches to $-V_{sat}$ and remain at this level as long as V_{in} is greater than V_{UT} . For $V_{02} = -V_{sat}$, the feedback gain will be $-\beta V_{02}$, when the input voltage V_{in} becomes lesser than V_{LT} , causes V_{02} to switch from $-V_{sat}$ to $+V_{sat}$. The difference between these two voltages is the hysteresis width V_H .

Using nodal analysis and current-voltage characteristics of CCCII as specified in (1), the expression for the output

voltage can be solved as given below:

The input current at terminal X is:

$$I_{in} = \frac{V_{in} - V_X}{R_1} \quad (4)$$

The input current at terminal Y is:

$$I_Y = \frac{V_{02} - V_Y}{R_2} \quad (5)$$

Solving the above equations using (1), the expression for V_{UT} and V_{LT} are derived as below:

The upper threshold voltage is expressed as:

$$V_{UT} = \frac{R_2}{R_1 + R_2 + R_B} (+V_{sat}) \quad (6)$$

The lower threshold voltage is expressed as:

$$V_{LT} = \frac{R_2}{R_1 + R_2 + R_B} (-V_{sat}) \quad (7)$$

Using additional current mirror configuration, square wave output with 180° is obtained at output terminal V_{01} . The hysteresis voltage shifts in between $+V_{sat}$ and $-V_{sat}$ and graphically shown in Fig. 4. Hysteresis is indicative of noise effect and delay appearing in the output signal. As value is lowered, the better would be the performance of the device [6]-[9].

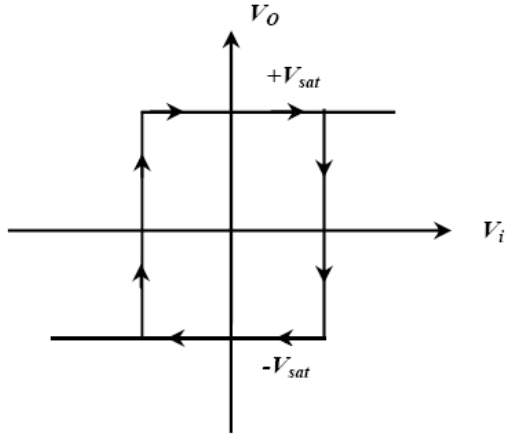


Fig. 4. Hysteresis phenomenon for the proposed circuit Fig. 3

Non-Ideal Analysis

Taking into consideration of non-idealities of the CCCII, the basic equation (1) can be expressed as:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ \alpha & R_B & 0 \\ 0 & \beta & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (8)$$

where $\alpha = 1 - \varepsilon$, $|\varepsilon| \ll 1$ represents the tracking error of voltage and $\beta = 1 - \delta$, $|\delta| \ll 1$ is the tracking error of current.

Using the small signal analysis, the voltage transfer gain α and current transfer gain β are expressed as:

$$\alpha = \frac{V_X}{V_Y} = \frac{(g_{m2} + g_{m4})r_{02} \parallel r_{04}}{1 + (g_{m2} + g_{m4})r_{02} \parallel r_{04}} \quad (9)$$

$$\beta = \frac{I_Z}{I_X} = \frac{g_{m9}g_{m2}g_{m13} + g_{m4}g_{m12}g_{m11}}{g_{m9}g_{m12}(g_{m4} + g_{m12})} \quad (10)$$

The ideal value of α is unity and for balanced operation in the above equation, $g_{m13} = g_{m12}$ and $g_{m11} = g_{m19}$, if these conditions are applied then β is also unity.

Including the non-idealities the representation for the output voltage is expressed as:

$$V_{02} = \frac{\beta R_2 V_{in}}{R_1 + R_B + \alpha \beta R_2} \quad (11)$$

Further, the threshold voltage expressions are represented by

The upper threshold voltage is expressed by:

$$V_{UT} = \frac{\beta R_2}{R_1 + \alpha \beta R_2 + R_B} (+V_{sat}) \quad (12)$$

The lower threshold voltage by:

$$V_{LT} = \frac{\beta R_2}{R_1 + \alpha \beta R_2 + R_B} (-V_{sat}) \quad (13)$$

From the above equations it is clear that the presence of non-idealities does not effect the performance of the design and the effect of non-ideal gains can be ignored. It can be easily verified that equations (12) and (13) reduce to equations (6) and (7) as expected, for ideal CCCII± when $\alpha = 1$ and $\beta = 1$.

IV. SIMULATION RESULTS

The proposed Schmitt trigger in Fig. 3 has been simulated using PSPICE simulator. The internal schematic of CCCII was realized as specified in Fig. 2 by using $0.35 \mu\text{m}$ CMOS technology. The voltages $\pm V_{CC} = 2 \text{ V}$ and the value of dc biased current is $I_B = 50 \mu\text{A}$ ($R_B = 260 \Omega$) along with $R_1 = 1 \text{ k}\Omega$ and $R_2 = 10 \text{ k}\Omega$ are applied. The input signal frequency is 2 kHz and signal voltage $5 V_{p-p}$. The distinctive output waveforms at the output terminals V_{01} and V_{02} are illustrated in Fig. 5 and Fig. 6. The theoretical and simulated output voltages are matched depending on the upper and lower threshold voltages as derived previously. The frequency spectrum for the output voltage is shown in Fig. 7, it determines the range of frequency and above that the device works effectively.

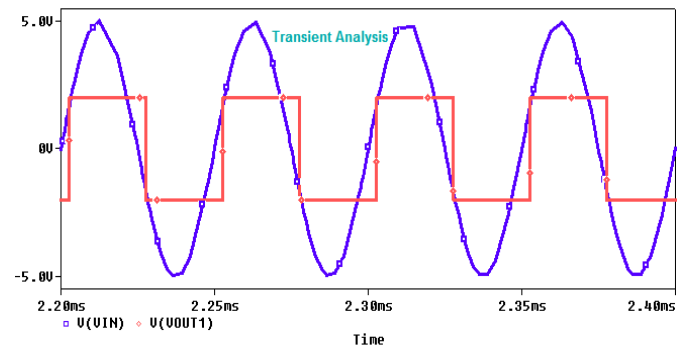


Fig. 5. The output waveform for the proposed Schmitt trigger at terminal V_{01}

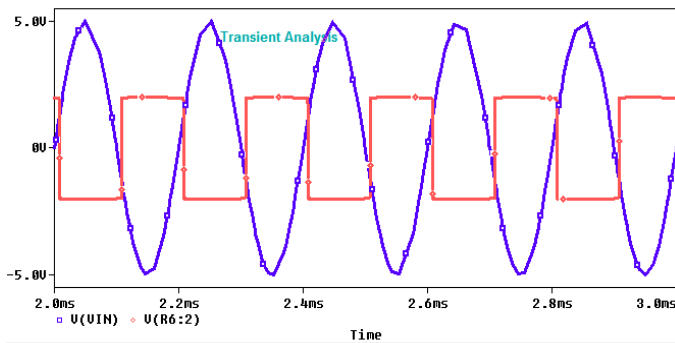


Fig. 6. The output waveform for the proposed Schmitt trigger at terminal V_{O2}

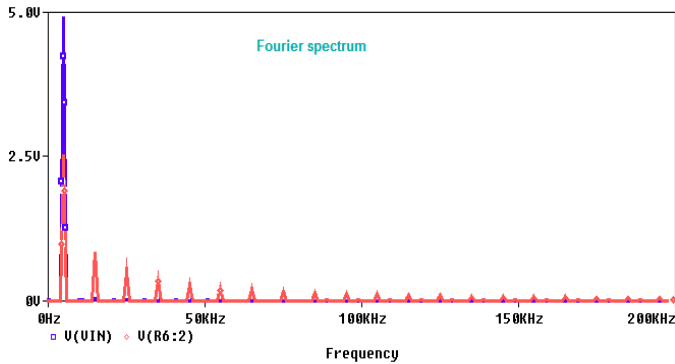


Fig. 7. Frequency spectrum of proposed Schmitt trigger

Montecarlo simulation is a technique used to measure uncertainty in the output signal. It is a technique that produces distributions of possible outcome values. The variable considered is resistance with a tolerance of 5% and run over for 50 iterations. Fig. 8 is the graph representing Montecarlo results for the proposed configuration. The mean value and standard deviation are 2.0017 and 0.000042 respectively which are quite low and suitable for better performance of the circuit. Fig. 9 represents the worst-case analysis for the proposed configuration. This analysis is used to identify the most critical components which will affect the circuit performance. It is accomplished by setting all the resistance values to their peak tolerance limits which gives the indication of the worst case results. For the proposed configuration the graph in Fig. 9 represents the least variation of output voltage with respect to the 5% variation in the tolerance of the resistance of Schmitt trigger circuit.

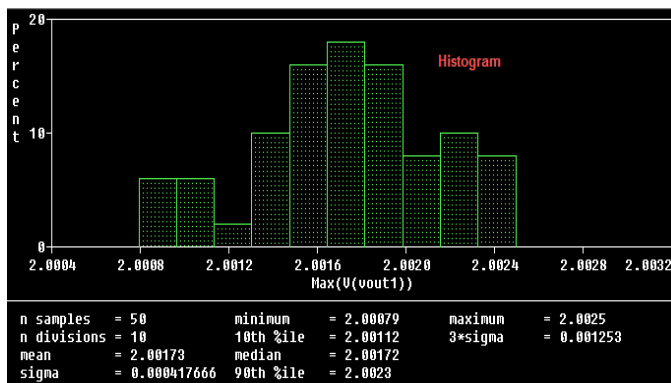


Fig. 8. Histogram for the output signal-1 of the proposed Schmitt trigger

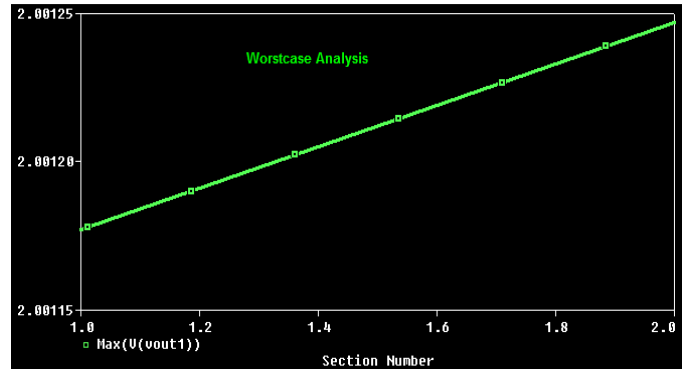


Fig. 9. Worst-case Analysis for the output signal V_{O1} of the proposed Schmitt trigger

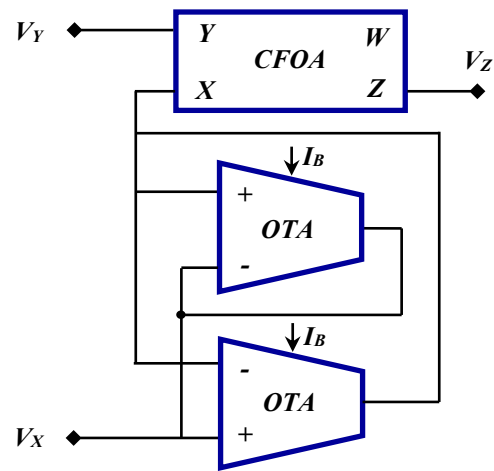


Fig. 10. Prototype of CCCII using CFOA and OTA

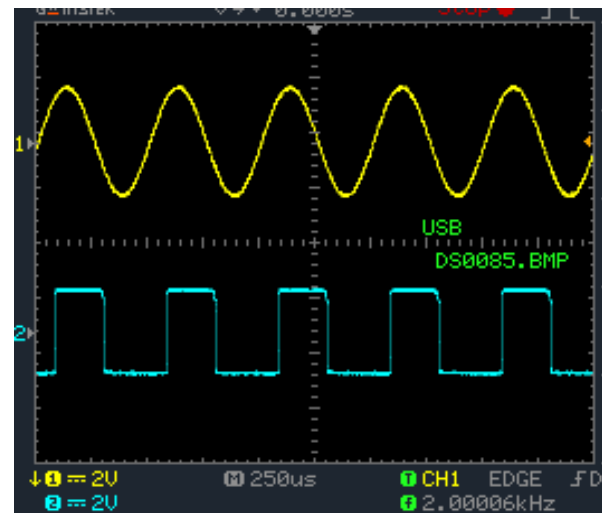


Fig.11. Experimental results of the proposed Schmitt trigger at V_{O1} of Fig. 3 on oscilloscope (Scale X-axis 250 μ s/div and Y-axis 2 V/div)

V. EXPERIMENTAL RESULTS

CCCII prototype is implemented using the structure shown in Fig. 10 [21]. The hardware implementation of the proposed design is done on laboratory bread board with commercially available current feedback operational amplifiers (CFOA), IC

AD844AN [33] and operational transconductance amplifiers (OTA), IC LM31700 [34]. The resultant output waveforms are included in Fig. 11 and Fig. 12. The output result shown in Fig. 11 is represented by V_{o1} , where as for the output indicated in Fig. 12 is by V_{o2} for the specifications of $R_1=1k\Omega$, $R_2=10k\Omega$, $I_B=100\mu A$ and input signal frequency of 2 kHz with $2V_p$. The experimental results determine that the proposed Schmitt trigger is best suited to perform the hysteresis operation and is represented graphically in Fig. 13.

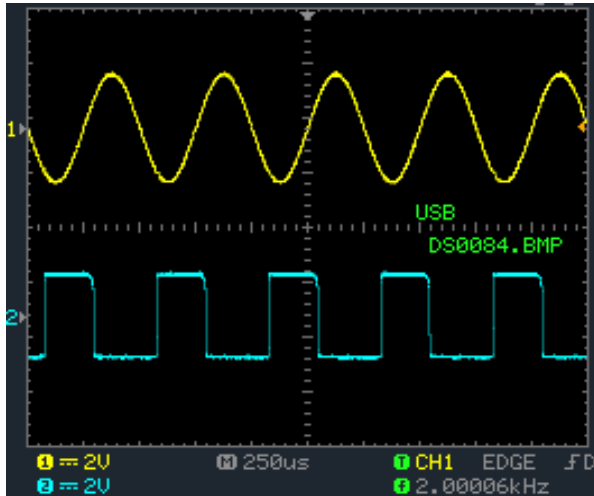


Fig.12. Experimental results of the proposed Schmitt trigger at V_{o2} of Fig. 3. on oscilloscope (Scale X-axis 250 μs /div and Y-axis 2 V/div)

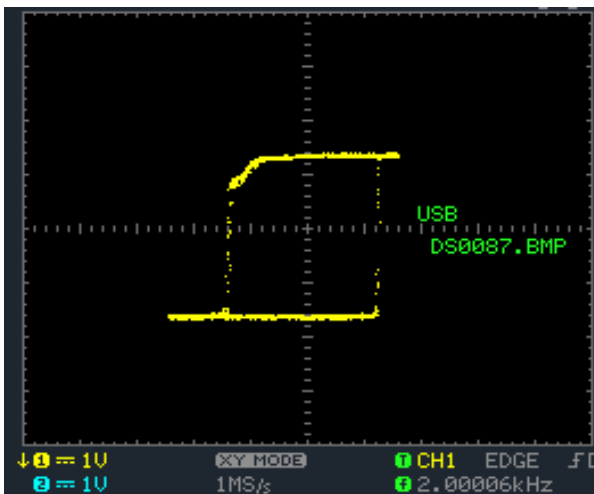


Fig. 13. Hysteresis phenomenon for the proposed Schmitt trigger.

The design involving dual output Schmitt trigger is mainly focussed on utilizing lesser number of active elements and passive components. Many topologies are available in the literature on Schmitt triggers and some of the topologies of our interest are listed in the comparison Table I. The configurations of [4] and [5] utilizes more number of active elements whereas, the circuits of [4], [5], [13] and [20] have more number of passive components involved in realization. The common drawback is that number of active and passive elements occupies more area and thereby large power consumption. Usually, these types of topologies are less preferred for IC fabrication. The structure of [22] has the advantage of having a single active device with no resistors. It suffers from certain drawback by having 28 MOS Transistors for its realization and able to produce single output. Whereas, the proposed configuration finds the advantage of utilizing single CCCII along with only two resistors for realization and is able to produce dual outputs. It can be applied as waveform generator, pulse width modulator, multivibrators e.t.c. It can also be utilized in realizing many electronic circuits. It is also well suited for IC fabrication.

VI. CONCLUSION

In this manuscript, a current mode dual output Schmitt trigger topology using CCCII is presented. The circuit has only two resistors and a CCCII as an active element, which is more advantageous for IC fabrication. Simulation results verifying theoretical analysis are included along with frequency spectrum. Montecarlo analysis and worst-case analysis are determined. Hardware results of the proposed design are obtained which are in similarity with the software results. The comparative analysis of the proposed topology is made with the existing methods. The reported topology has simple structure that requires less active and passive components, thereby, less area and offers low power dissipation than the other similar technologies.

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TABLE I. STATE OF ART COMPARISON OF PROPOSED DUAL OUTPUT SCHMITT TRIGGER

Reference	Active Element	Number of Active Elements	Number of Passive Elements	Number of Resistors	Single/ Dual output
[4] Jiri Misurec <i>et.al</i>	CCII	2	4	4	Single
[5] A. Srinivasulu	CCII	2	4	4	Single
[13] S. Minaei <i>et.al</i>	DVCC	1	2	2	Single
[14] Y. K. Lo <i>et.al</i>	OTRA	1	1	1	Single
[20] M. Faseehuddin <i>et.al</i>	DOCCII, Inverter	1, 1	2	2	Single
[22] A. Kumar <i>et. al</i>	DXCCTA	1	0	0	Single
Proposed Circuit of Fig. 3	CCCII	1	2	2	Dual

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