A Full Adder Design with CNFETs for Real Time, Fault Tolerant and Mission Critical Applications

Jitendra Kumar Saini, Avireni Srinivasulu, and Renu Kumawat

***Abstract*—The VLSI based circuits often pose challenges in the form of various faults (such as transient faults, permanent faults, stuck-at-faults). These faults appear even after testing also. They occur because of reduction in the size of the circuit or during real-time implementation, as these faults are difficult to detect. It is very important to detect and rectify all such faults to make the system foolproof and achieve expected functionality. In this paper, 12 transistors based, full adder circuit (12T-FAC) using Carbon Nanotube Field Effect Transistor (CNFET) technology is proposed. The proposed design based on CNFET provides high fault resistance towards transient, permanent faults and works with least power, delay and power-delay product (PDP). Later, features like fault detection and correction circuit have been added in 12T-FAC. The final version of full adder circuit capable of correcting errors has been used in designing applications like multipliers. The proposed full adder circuit was designed with CNFET technology, simulated at 32 nm with supply voltage +0.9 V using the Cadence Virtuoso CAD tool. The model used is Stanford PTM.**

***Keywords*—CNFET, Full Adder, Fault Detection Full Adder, Fault Correction Full Adder, Multiplier.**

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I. Introduction

INIn the real-time circuits, it is crucial to identify faults else the outcome may be catastrophic for the system and may even claim human lives too. While designing circuits for these applications, fault detection and fault correction have played a crucial role and posed challenges [1]. As Moore's Law states, "The number of transistors in dense integrated circuit doubles every two years", and hence leads to the growth of complexity. The efforts to bring down the size of the circuits have also made the later prone to certain faults like crosstalk, noise, etc. There are other setback issues which remain undetected during the initial testing. These issues are often difficult to detect and more concerned for its rectification and therefore the majority of the researchers usually concentrate on the identification and rectification of such issues [2]. The integrated circuits can be designed using various components like adder being the most common among the preferred by the designers. An adder is the simplest component capable of executing an arithmetic operation. It can be used to design various similar arithmetic and logical circuits [3].

The applications where carbon nanotubes may be used are antennas, invasive nanobots, miniaturized satellites, and Geo-positioning systems [4]. But there are applications where an alternate to resistors may work more effectively in optics based devices wherein Chlorophyll like organic semiconductors such as phthalocyanines (CuPc) with good thermal stability, chemical stability, light resistance, temperature resistance, coating strength and resistance to bases is preferred [4]-[5]. Some such applications are temperature sensors, humidity sensors, photo detectors, solar cells, optoelectronic devices, radio frequency identification, etc [5]. For these applications, the real-time systems need on-the-fly fault detection and correction circuits to make a system truly fault-tolerant. [5]

In VLSI, adders are used extensively and hence while designing a circuit using CNFET [6], adders are an obvious choice.

Carbon nanotube (CNT) is an allotrope of carbon with a cylindrical structure. The structure is found to be either single-walled carbon nano tube (SWCNT) or multi-walled carbon nano tube (MWCNT). SWCNT is a single sheet rolled up cylindrically along a wrapping vector $C = n_1\mathrm{a} + n_2\mathrm{b}$, where n_1 and n_2 are positive integers which specify the Chirality of the tube, and 'a' and 'b' are lattice unit vectors, as shown in Fig. 1.

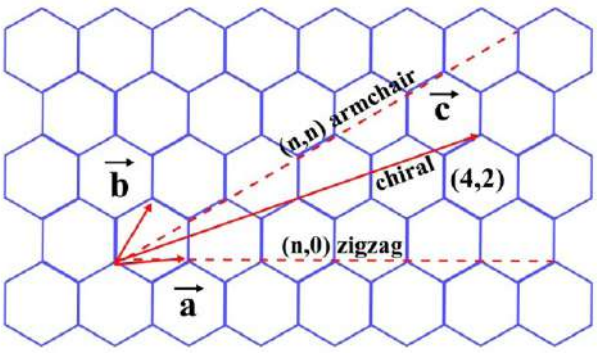

Fig. 1. A spread-out sheet of graphite and Chirality of the CNT tube [8]

Depending upon the value of n_1 and n_2, SWCNT can be either metallic or semiconducting. If the n_1-n_2 is a multiple of 3,

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SWCNT is metallic or else it is semiconductor.Further classification of SWCNT includes armchair CNT ($n_1 = n_2 = n$), zigzag CNT ($n_1=n$, $n_2 = 0$) and Chiral CNT ($n_1 \neq n_2$ and n_1, $n_2 \neq 0$). The armchair CNTs conductors while zigzag and Chiral CNT's act as either semiconductor or conductor depending upon the difference in indices (i.e. n_1-n_2) [7]-[8].

The expression for the threshold voltage (V_{th}) [7], equivalent to half the band gap of CNFET is shown in (1):

$$V_{th} \approx E_{bg} / 2e \approx 0.436 / D_{CNT}(nm) \quad (1)$$

Where the E_{bg} is the band gap of CNFET, e is the electron charge, D_{CNT} is the diameter of carbon nanotubes as given in (2):

$$D_{CNT} = d \approx 0.0783\sqrt{n_1^2 + n_2^2 + n_1 n_2} \quad (2)$$

The thermal efficiency (Z) of the circuit as given in (3) is improved using nano-structuring and bandgap engineering by reducing the lattice thermal conductance and enhancing the Seebeck coefficient [9]. CNT based applications typically offer superior potential where the CNTs increase the power factor with increasing temperature [9].

Efficiency (Z) is calculated from expression [10]:

$$Z = \frac{\sigma\alpha^2}{K} \quad (3)$$

where, σis the electrical conductivity, k is the thermal conductivity and α is the Seeback coefficient. Later a dimensionless figure of merit came into existence which is calculated as ZT.

Temperature (T) as shown in (4) is calculated from expression [10]:

$$T = \frac{T_1 + T_2}{2} \quad (4)$$

where, T_1 and T_2 are the temperature of two contacts. The above equations are applicable for fabricating power generation devices using Bi_2Te_3 and CNT along with silicon adhesive.

Section II and III of theresearch article discuss the existing full adder circuit designs and fault tolerant circuit designs approaching all along the drawbacks. Section IV discusses the proposed design. Section V gives the simulation results, comparative details and finally Section VI give concluding remarks.

II. Existing Full Adde r Circuit Designs

The conventional full adder design [3] consists of 28 transistors and has a larger propagation delay due to the presence of 5 transistors in the output data path. Transmission Gate Adder (TGA) works on transmission gate logic, has a transistor count of 20 and critical data path delay of 4 transistors. This design has a drawback in driving capability [3]. Transmission Function Adder (TFA) carrying 16 transistors works on the principle of the transmission function theory. Similarly TGA and TFA also suffer in its driving capabilities [11].

In the case of Complementary Pass-transistor Logic Transmission Gate (CPL-TG), this design has better driving abilities but however it uses more transistors [12]. Mirror full adder design is an alternative to C-CMOS based full adder circuit. Mirror adder uses Pass Transistor Logic (PTL) approach that has a critical path of 4 transistors. Thus, it results in faster full adder design and lower power delay product along with a high transistor count [13]. Static Energy Recovery Full Adder (SERF) uses only 10 transistors, but suffers from a threshold loss of problem [14]. The 13A full adder circuit uses 10 transistors similar to SERF full adder design and suffers from a specific problem of output voltage level degradation [15]. Hybrid Pass Transistor Logic with Static CMOS output drive (HPSC) full adder is designed using transmission gate logic, pass transistor logic and CMOS logic with a transistor count of 26 [16]. NEW-HPSC full adder consists of 24 transistors and has higher power consumption because it has one extra inverter in the full adder design [17]. Complementary and level restoring carry logic full adder (CLRCL) is based on pass transistor logic and uses only 10 transistors. In this case, power consumption is more due to the presence of inverter circuit in the design of a full adder [18]. The Ours1 full adder consists of double pass-transistor logic (DPL) and that uses 28 transistors in the circuit of full adder. This design suffers from poor driving capability [19]. Hybrid CMOS logic with transmission gate logic full adder (HCTG) consists of 16 transistors and has a critical path delay of 4 transistors. One important drawback in HCTG is that it is not suitable for cascaded stages because it has poor driving capability due to the coupling of inputs and outputs [20]. Removed Single Driving Full Adder (RSD-FA) consists of 26 transistors. This design has an XOR/XNOR circuit that exhibits full driving capability and output delay path of 4 transistors. RSD-FA provide lower power consumption as well as the high speed at the cost of more transistor count [21]. In 1-Bit full adder with 18 transistors [22], five inverters are used that is three at primary inputs and 2 in the intermediate stage which results in poor driving capability. Hybrid Multi-Threshold Full Adder (HMTFA) consists of 23 transistors. Provides Critical path of 4 transistors and experience a threshold problem due to the use of more number of inverters [23].

Literature review of full adders has been verified with different logic families. They are found to vary in their characteristic features, performance, power consumption and propagation delay. The crucial points undermining the approximation and comparison of performance among the devices are delay, power consumption, and power-delay product. Circuit delay along with other factors is largely on account of number of transistors consecutively connected in series all along the channel width and intra-cell wiring capacitances. Similarly, size is directly proportional to the number of transistors and results into complexity while implementation. Thus, by reducing the number of transistors, we can optimize the circuit performance in terms of area and speed.

This paper demonstrates the improvement in circuit performance by reducing the number of transistors and length of the critical path of outputs. One-bit full adder circuit using 12 CNFETs (denoted as 12T-FAC) has been proposed in this paper. In the proposed full adder circuit, care has been taken to minimize the limitations of the earlier proposed full adder and also to improve the overall circuit performance.

III. Existing Fault-Tolerant Circuit Designs Approach

Any fault tolerant system needs to acquire few characteristics by virtue of its design, existing design approaches like redundancy (time, hardware), etc. are summed up to get the features at a glance. Here on Time Redundant design approach deals with fault detection by executing the same operation on two circuits which are identical and at times by adding latency in the input feed of one of the circuits and compare the output thus obtained, where the same output represents no fault and the difference of output represents a defaulted circuit [1]. The Hardware Redundancy design approach requires multiple instances (two, three or more) of the identical circuits with common input feed giving out different results [2]. Operand Width Aware Hardware Reuse design approach uses the combination of the static and dynamic (redundant) adder to design ALUs. The Self-Checking Carry Select Adder design [24] approach detects single bit fault at run time and also capable of detecting a stuck-at fault. Self-Repairing Adder [25] design approach makes use of a pre-defined rule which says, "For 3 input adders, same input values should produce the same output values and if any of the input is flipped, the output differs". The Real-Time Fault Tolerant Full Adder design approach moves one step ahead and is capable of detection and correction of single and double faults at run time [26].

Every technique has got its own advantages and disadvantages like time redundant design approach is unable to detect faults if the results of the initial input feed are incorrect [27]. This approach does not detect stuck-at-faults. In hardware redundant design approach real-time faults and stuck-at faults may not be possible to detect, hence correction circuit cannot be designed, and also there will be a drasticincrease in size of the circuit [28]. In Operand Width Aware Hardware Reuse design approach the computational complexity, power consumption, and fault propagation are the challenges that designers need to address [29]. The Self Checking Carry Select Adder design approach [30] suffers from a probable handicap to detect the fault site if there are multiple faults detected in the circuit. It also restricts its use in self-correcting circuits. The Self Repairing Adder design approach [31] fails while multiple wrong inputs are provided to the adder and are unable to identify the location. In Real-Time Fault-Tolerant Full Adder design approach the number of hardware components is high due to redundancy in design and thus are more costly [32]-[33]. Due to the redundant circuit design, critical path delay is increased and thereby increases the overall circuit delay [34]-[38].

The proposed design of full adder circuit (12T-FAC) along with error detection and correction circuit mechanism deals with delay, reduces the redundant components, identifies stuck-at-fault, can also detect multiple fault locations and is capable of fault corrections. Hence, fabrication of the proposed design, true real-time fault tolerant circuit design can be achieved [39]-[42].

IV. Proposed Design

The proposed system is verified on the basis of the criteria given below:

1) ***Test Strategy:*** We have tested the output under two functional units considering each output (Sum and Carry) to be independent of the other. This strategy allows us to trace back the fault location.
2) ***Hardware Design:*** The circuit reduces the need for redundant adders and it does not make use of multiple rail checkers which allows a comparatively lean hardware design.
3) ***Fault Detection:*** Proposed design is fully capable of fault detection and fault correction in case of sporadically occurring transient and other permanent faults.

The block diagram of the proposed 1-bit adder circuit as represented in Fig. 2 contains three blocks, wherein,*Block-A* takes input A and B to produce intermediate output as XOR/XNOR signal pair. This block is implemented using transistors C_1, C_2, C_3, C_8, C_9, and C_{10}. *Block-B* is a Pass Transistor Logic implementation that takes intermediate output XOR/XNOR as input along with initial carry C_{in} (if any) and generates output Sum. *Block-B* is implemented using C_4, C_5, C_6, and C_{11}. *Block-C* is a multiplexer that takes A, XNOR, and C_{in} as input and produces Carry as output. *Block-C* is implemented using transistors C_7 and C_{12}.

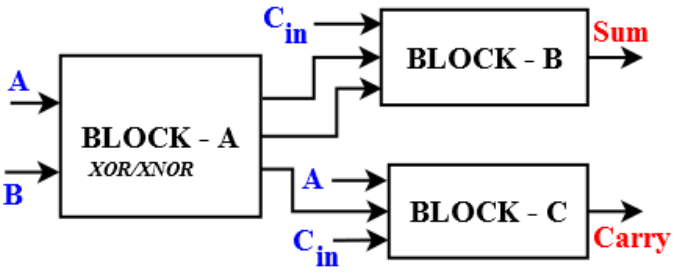

Fig. 2. Block diagram of proposed 12T-FAC

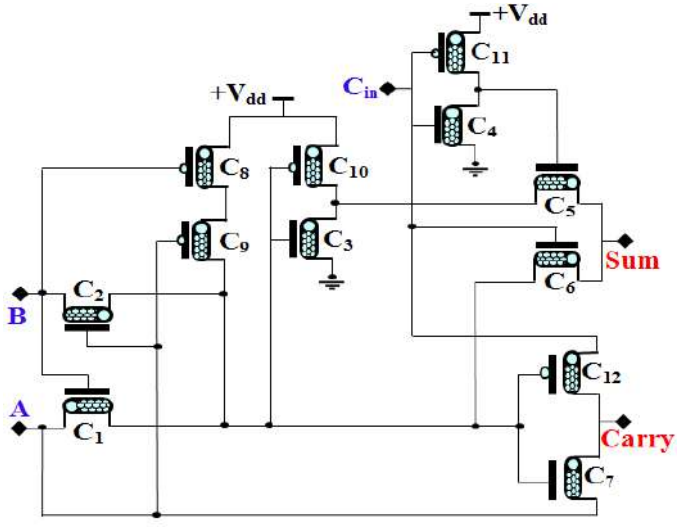

Fig. 3. Schematic of proposed 12T-FAC implemented using CNFET.

The proposed 12 transistors full adder circuit using CNFET is shown in Fig. 3. The proposed 12T-FAC circuit has a critical path delay of 3 and provides full output voltage swing. The Sum and Carry equation of 12T-FAC are:

$$\text{Sum} = \text{A} \oplus \text{B} \oplus \text{C}_{in} \tag{5}$$

$$Sum = \overline{A}\,\overline{B}C_{in} + \overline{A}\text{B}\overline{C_{in}} + \text{A}\overline{B}\,\overline{C_{in}} + ABC_{in} \tag{6}$$

$$\mathbf{Sum = (AB + \overline{A}\,\overline{B})C_{in} + (A\overline{B} + \overline{A}B)\overline{C_{in}}} \tag{7}$$

$$Carry = (A\overline{B} + \overline{A}\text{B})C_{in} + \text{A}(\overline{A}\,\overline{B} + AB) \tag{8}$$

$$\mathbf{Carry = (A\overline{B} + \overline{A}B)C_{in} + AB} \tag{9}$$

Using (2) the value of D_{CNT} was calculated keeping the value of $n_2 = 0$ and varying value of n_1 in the range of 7-19 with step size 2.

$$D_{CNT} = 0.0783 * n_1 \tag{10}$$

Similarly, using (1) and the various D_{CNT} values, the value of V_{th} was calculated as

$$V_{th} = 0.436 / D_{CNT} \tag{11}$$

Using 12T-FAC, theFault Detection Full Adder (FDFA) circuit based on CNFET is proposed. This circuit is capable of detecting multiple faults (single and double) in real-time along with identification of fault site. The schematic of the FDFA is shown in Fig. 4.

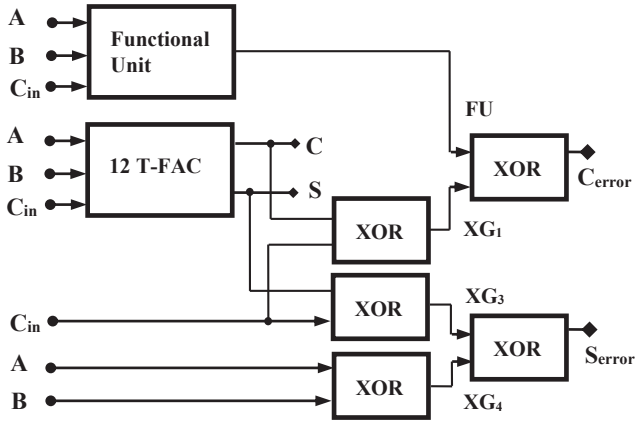

Fig. 4. Schematic of FDFA

Proposed FDFA makes use of 3 input (A, B, C_{in}) and generates 4 output (S, C, S_{error}, C_{error}) where S and C denotes actual results (i.e. Sum and Carry) of FDFA and S_{error} and C_{error} verifies whether there is an error in the sum or carry outputs of FDFA respectively. C_{error} is generated by XOR of XG_1 and Functional Unit (FU) given in (12) whereas, intermediate output stage FU and XG_1 are shown in (12) and (13) respectively.

$$\text{FU} = \overline{(\text{A} + \text{B} + \overline{\text{C}_{in}})(\overline{\text{A}} + \overline{\text{B}} + \text{C}_{in})} \tag{12}$$

$$\text{XG}_1 = \text{C} \oplus \text{C}_{in} \tag{13}$$

$$\mathbf{C_{error} = FU \oplus XG_1} \tag{14}$$

When C_{error} = '0', indicates fault-free FDFA circuit while C_{error} = '1', indicates the faulty FDFA circuit and the fault site is the carry output stream.

Similarly, in regards to the detection of a fault, if fault site is in the sum output stream that requires 3 XOR gates. S_{error} is generated by XOR of XG_3 and XG_4 shown in (17) whereas, intermediate output stage XG_3 and XG_4 are shown in (15) and (16) respectively.

$$\text{XG}_3 = \text{C}_{in} \oplus S \tag{15}$$

$$\text{XG}_4 = \text{A} \oplus \text{B} \tag{16}$$

$$\mathbf{S_{error} = XG_3 \oplus XG_4} \tag{17}$$

When S_{error} = '0', indicates fault-free FDFA circuit, while S_{error} = '1', indicates the faulty FDFA circuit and the fault site is the sum output stream. These would make it capable of detecting single or multiple faults occurring in sum and carry bits and when no error occurs, then S_{error} and C_{error} will remain Zero representing fault free FDFA.

Once the fault site is identified, the proposed FDFA makes use of Fault Correction Full Adder (FCFA) for recovery of erroneous input in real-time. This circuit design deal with all the sporadically occurring transient faults and permanent hardware faults thus make the circuit a real fault-tolerant design.

In this approach, an inverter is used along with multiplexer to correct the output sum and carry, instead of using standby adder to replace the faulty adder as is used in earlier approaches. This substantially reduces the hardware size to a fraction as compared to the other existing design approaches. The schematic of the FCFA is shown in Fig. 5.

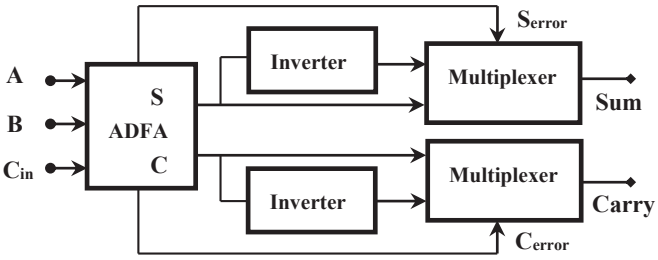

Fig. 5. Schematic of proposed FCFA.

The output (S and C) generated by the 12T-FAC from input (A, B, C_{in}) is fed to the FDFA circuit which produces output (S, C, S_{error} and C_{error}) to be further fed to FCFA, which takes S, C and their complements as input and passes to the Multiplexer where S_{error} and C_{error} are used as select line, depending upon the detection of error output the Sum and Carry are selected.

If the outputs S_{error} and C_{error} are 0, then the S and C outputs of FDFA are directly transferred as final Sum and Carry of FCFA with the help of multiplexer and if S_{error} and C_{error} of FDFA are 1, then the inverted outputs received from the inverter gets selected by multiplexer and are transferred as final Sum or $\overline{\text{Sum}}$ and Carry or $\overline{\text{Carry}}$ of FCFA.

V. Simulation Results And Comparison

The simulation is carried out using the Cadence Virtuoso Tool. The circuit is designed with CNFET 32 nm technology [43] at Supply Voltage ($+V_{dd}$) 0.9 V. The waveform of the 12T-FAC consists of inputs (A, B, C_{in}) and outputs (Sum and Carry) are shown in Fig. 6.

TABLE I
Comparison Between Proposed 12T-FAC And Other Full Adders in Terms of Transistor Count, Delay, Power and PDP.

Full Adder	Transistor Count	Power (µW)	Delay (ps)	PDP (aJ)
C-CMOS [3]	28	0.124	12.355	1.532
TGA [3]	20	0.135	10.104	1.364
TFA [11]	16	0.109	11.701	1.275
SERF [14]	10	3.326	9852.7	32770.0
13A [15]	10	5.819	9507.8	55325.8
NEW-HPSC [17]	24	0.123	30.232	3.718
CLRCL[18]	10	5.903	231.18	1364.6
RSD-FA [21]	26	0.091	9.427	0.857
18T-FA [22]	18	0.088	8.93	0.785
HMTFA [23]	23	0.121	16.909	2.056
This work	12	0.039	6.876	0.268

The simulation results of all the full adders as reported in Section 2 and proposed 12T-FAC are summarized in Table I. However, the supply voltage ($+V_{DD}$) is varied in the range of 0.6 V to 1.4 V with a step size of 0.1 V to verify the fault tolerance of the circuit in varying voltage scenario. It was observed that the proposed circuit performs consistently under variations in various parameters, as could be seen in Table II.

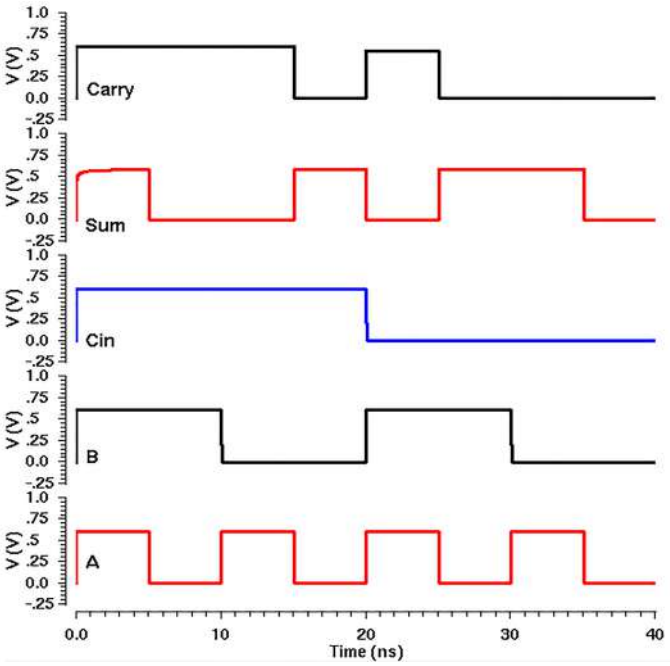

Fig. 6. Waveform of proposed 12T-FAC using CNFET

TABLE II
Comparison of proposed 12T-FAC design in terms of variation in V_{DD} Supply from 0.6 V to 1.4 V for 32 nm CNFET Technology with Vth = 0.289 V.

Proposed Full Adder	V_{DD} (Volts)	12T-FAC
Average Power	0.6	0.018 µW
	0.7	0.022 µW
	0.8	0.029 µW
	0.9	0.039 µW
	1.0	0.059 µW
	1.1	0.076 µW
	1.2	0.095 µW
	1.3	0.119 µW
	1.4	0.166 µW
Delay	0.6	9.353ps
	0.7	8.019ps
	0.8	7.821ps
	0.9	6.876ps
	1.0	6.772ps
	1.1	6.701ps
	1.2	6.559ps
	1.3	6.498ps
	1.4	6.339ps
PDP	0.6	0.168aJ
	0.7	0.176aJ
	0.8	0.227aJ
	0.9	0.268aJ
	1.0	0.400aJ
	1.1	0.509aJ
	1.2	0.623aJ
	1.3	0.773aJ
	1.4	1.052aJ

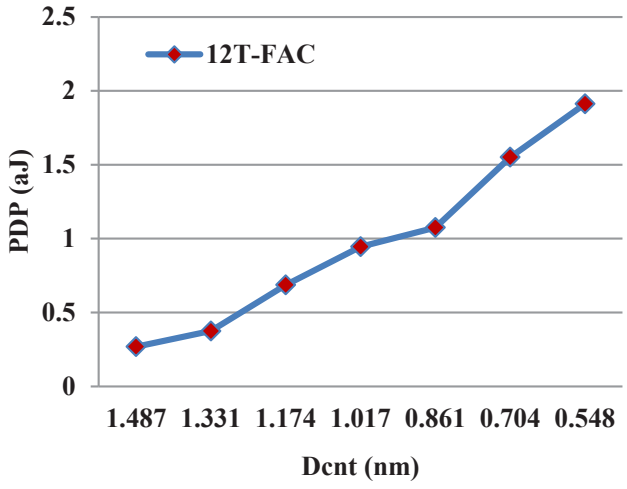

Fig. 7. PDP Versus Dcnt Variations for proposed circuit

The results from (10) and (11) are used to plot parameter variation of power-delay product (PDP) of 12T-FAC with CNFET diameter (D_{CNT}) and threshold voltage (V_{th}) as shown in Figs. 7 and 8, respectively.

The CNT structure used is SWCNT in Zigzag orientation where (n_1 = n, n_2 = 0). For simulation and study purpose, the value of n1 was varied in the range of 7 to 19. Significant PDP results were observed at n_1 = 19 and hence the value was used for further comparisons. Other CNFET parameters used during the simulation are shown in Table III.

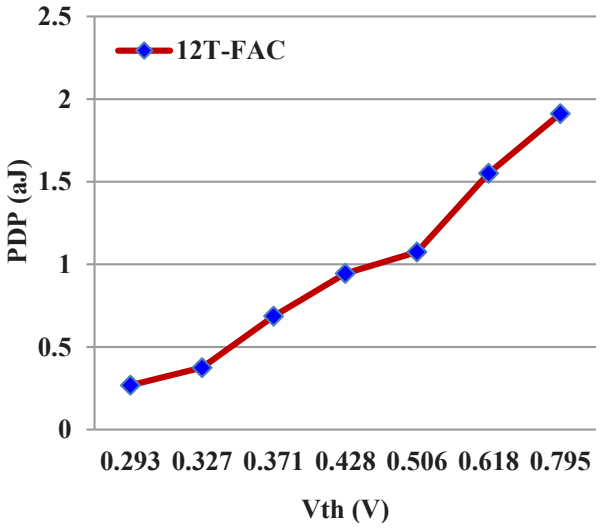

Fig. 8. PDP Versus Vth Variations for proposed circuit.

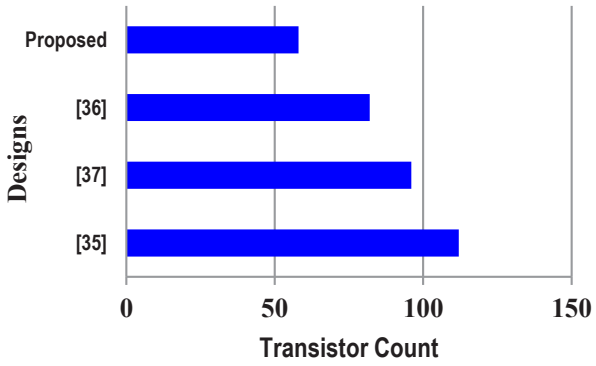

Fig. 9. Comparison of fault tolerant design with transistor count.

TABLE III
CNFET DESCRIPTION, VALUE AND ITS PARAMETER.

Description	Value	CNFET Parameter
Physical channel length	32 nm	Lg
The mean free path in the intrinsic CNT channel	200 nm	Lgeff
The length of doped CNT source-side extension region	32 nm	Lss
The length of doped CNT drain-side extension region	32 nm	Ldd
The Fermi level of the doped S/D tube	6 EV	Efi
The dielectric constant of high-k top gate dielectric material	16	Kgate
The thickness of high-k top gate dielectric material	4 nm	Tox
The coupling capacitance between the channel region and the substrate	20 pf/m	Csub
Distance between the tubes	20 nm	Pitch
Zigzag Structure	19	n1
	0	n2
Number of CNT tubes	3	CNTPos

The impact of temperature variations on the proposed 12T-FAC circuit was observed from the simulations for the temperature range -50°C to 150°C. The simulated temperature stability was observed to be 0.00000035%, as shown in Fig.10.

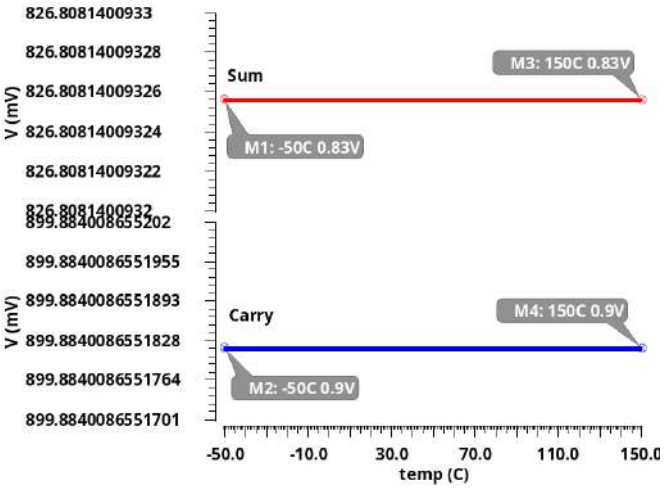

Fig. 10. Simulated temperature stability 12T-FAC

The static power consumption is determined by the clock and all other inputs that are connected with the low logic to check the leakage current.

The dynamic power dissipation is calculated using switching frequency and external load capacitance from relation [5]:

$$P_{dynamic} = \alpha C_L f V_{DD}^2 \quad (18)$$

where α ($0 \le \alpha \le 1$) is switching activity factor, f is the clock frequency and C_L is the load capacitance. The frequency and capacitance are directly proportional to the dynamic power consumption.

To find the static power and leakage current, V_{DD} = 0.9V is supplied with low level inputs (*A, B, Cin*), whereas to calculate total power consumption V_{DD} = 0.9 V is supplied with inputs (*A, B, Cin*). When these parameters were applied to simulate the proposed 12T-FAC leakage current, static power, dynamic power, and total power recorded were 0.275 nA, 0.256 nW, 38.979 nW, and 39.235 nW, respectively.

The average power consumption of 1-bit FCFA was found to be 9.81 nW and delay was 5.382 ps. The power-delay prod-

uct was 0.0528 aj. The circuit thus designed when simulated along with existing designs, was found to be at-par in terms of capabilities like fault detection and fault correction. Also, it is evident that the proposed design reduces the number of transistors by 30% and the size by 45% approximately as depicted in Fig. 9.

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The mean free path in the intrinsic CNT channel	200 nm	*Lgeff*
The length of doped CNT source-side extension region	32 nm	*Lss*
The length of doped CNT drain-side extension region	32 nm	*Ldd*
The Fermi level of the doped S/D tube	6 EV	*Efi*
The dielectric constant of high-k top gate dielectric material	16	*Kgate*
The thickness of high-k top gate dielectric material	4 nm	*Tox*
The coupling capacitance between the channel region and the substrate	20 pf/m	*Csub*
Distance between the tubes	20 nm	*Pitch*
Zigzag Structure	19	*n1*
	0	*n2*
Number of CNT tubes	3	*CNTPos*

Table IV gives the capability comparison with the existing design approaches. At the time of simulation, it has been observed that the proposed circuit of FCFA is successfully able to auto correct the error, if any. From Fig. 11, it can be seen that the input sequence (A, B, C_{in}) without any error (S_{error}=C_{error}=0) gives expected output for various input combinations.

TABLE IV
CAPABILITY COMPARISON WITH EXISTING DESIGN APPROACHES.

Designs	[31]	[33]	[32]	Proposed
Individual transistor count	2-Adder 56 4-XNOR 24 2-Eqt 24 2-Mux 08	1-Adder 28 2-XNOR 10 2 AND 14 1 OR 6 1-Fun.Unit 14 2-Mux 08 8-Inverter 16	1-Adder 28 5-XNOR 30 1-Fun. Unit 12 2-Mux 08 2-Inverter 04	1-Adder 12 5-XOR 20 1-Fun. Unit 18 2-Mux 04 2-Inverter 04
Total number of transistors	112	96	82	58
Fault coverage	Single net Multi net Single fault	Single net Multi net Single fault Double fault Stuck-at fault	Single net Multi net Single fault Double fault Stuck-at fault	Single net Multi net Single fault Double fault Stuck-at fault
Fault repairing	Not possible in case of double fault	Possible in all cases	Possible in all cases	Possible in all cases
Output reliability single fault	100%	100%	100%	100%
Output reliability double fault	85.82%	100%	100%	100%
Technology	CMOS	CMOS	CMOS	CMOS/ CNTFET

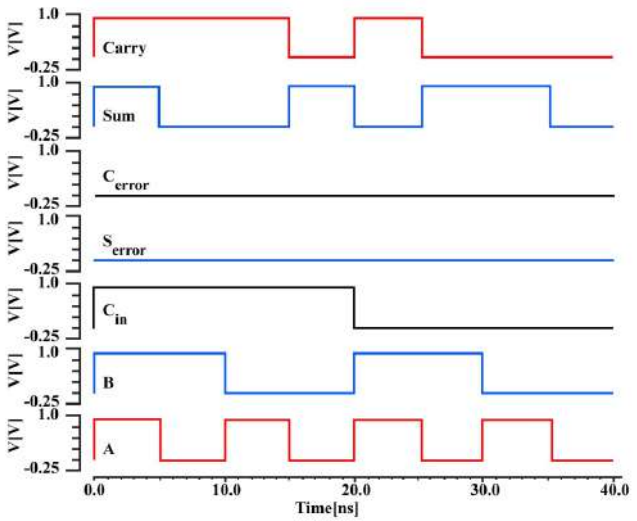

Fig. 11. Output waveform of FCFA with no error.

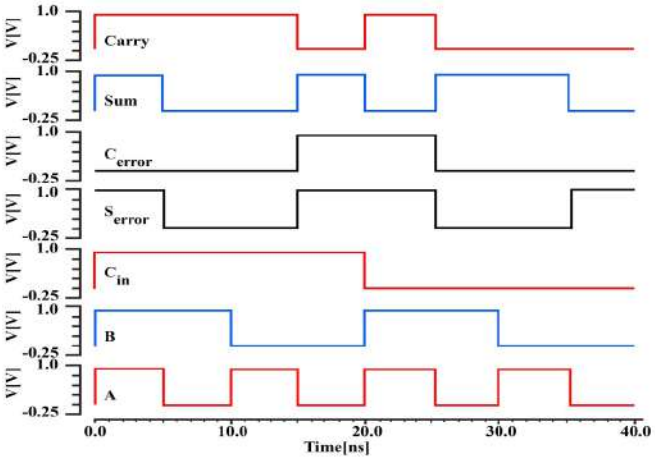

Fig. 12. Output waveform of FCFA with error correction in Sum and Carry

In Fig. 12, the observed output from input sequence (A, B, C_{in}) with fault detected in S_{error} and C_{error} of 12T-FAC shows the capability to auto correct the fault in final Sum and Carry. Further, to test the performance of FCFA in complex circuits, multiplier is designed in both CMOS and CNFET technology as dipicted in Table V.

TABLE V
COMPARISON OF MULTIPLIER DESIGNS.

Multipliers	Power (μW)	Delay (ps)	PDP (aj)	Technology (nm)
4 BIT Multiplier [32]	94.38	598.3	56467.6	CMOS 55
Proposed 4 BIT Multiplier CMOS	24.21	418.3	10127.0	CMOS 45
Proposed 4 BIT Multiplier CNFET	2.884	303.4	875.006	CNFET 32
8 BIT Multiplier [32]	712	1326	944112	CMOS 55
Proposed 8 BIT Multiplier CMOS	498	987.3	491675.4	CMOS 45
Proposed 8 BIT Multiplier CNFET	21.75	672.4	14624.7	CNFET 32

VI. CONCLUSION

In this paper, we have proposed a Full Adder Circuit (12T-FAC) using CNFET, Fault Detection Full Adder (FDFA) Circuit using CNFET, Fault Correction Full Adder (FCFA) Circuit using CNFET, 4-bit and 8-bit multiplier circuit using FCFA and CNFET.

The 12T-FAC is optimized to consume less power, having lesser delay and that too with less than the average number of transistors when compared with other similar designs. The proposed design is capable of performing all the tasks its peers are capable of. The FDFA and FCFA are the functionality extensions of proposed 12T-FAC to detect and correct the input/output. Finally, to test this circuit for its scope, capabilities, and worthiness, it was used to design a multiplier application.

It can also be seen from the simulation results that the Adders and Multipliers thus designed are producing better results as compared to other prevalent designs of a full adder. Table IV shows that the proposed ACFA design reduces the number of transistors required by 30% and the size by approximately 45%. Also, when the application (multiplier) was compared with other similar multiplier designs, the power consumption was found to be substantially low and so the delay. The proposed design deals with faults in real time and performs corrective action, this enables us to conclude that the proposed 12T-FAC is a better-suited design and a choice for future applications.

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