Sensitivity Analysis of the UTBSOI Transistor based Two-Stage Operational Amplifier

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Abstract—In the nanoscale domain, the MOSFETs are prone to various physical effects due to their shorter channel region known as short-channel effects (SCE). The researchers have proposed an advanced structure of MOSFET known as the ultrathin-body silicon-on-insulator (UTBSOI) to overcome the limitations of SCEs. The UTBSOI is a type of double-gate (DG) MOSFET having superior controllability of gates over the shorter channel region. Nowadays, the UTBSOI MOSFETs can be adopted in the circuit simulators through the use of a device model named BSIM-IMG. The BSIM-IMG has made it possible for the circuit designers to simulate any UTBSOI based analog blocks like operational amplifiers (opamp). The performance parameters of an opamp are very much sensitive to any perturbation in size (W/L) of the constituent MOSFETs, that may cause a drastic change in the output. In this paper, the sensitivity analysis procedure has been proposed for the CMOS and UTBSOI based two-stage opamps as the function of perturbation in W/L. In addition to this, an algorithm has also been presented to do the same. From the simulation results, it is observed that the sensitivity of the UTBSOI based opamp (UTBSOI-opamp) is larger than that of CMOS based opamp (CMOS-opamp).

Index Terms—Opamp, sensitivity analysis, UTBSOI.

I. INTRODUCTION

The operational amplifier (opamp) is a vital analog building block that is used in many circuits such as switched-capacitor filters, analog-to-digital converters, analog integrator and differentiator, etc. Many design techniques of the analog amplifiers [1]–[5] have been addressed in the literature so far. A design method, dynamic biasing (output impedance enhancement) technique [1], enhances the DC gain but reduces the settling of output [2]. The positive feedback technique [2], [3] also improves the DC gain without limiting its high-frequency performance, but here transistor matching is the main issue [6]. With the downscaling of technology nodes, the cascode topologies of the amplifiers [4], [5] have become less useful due to their limited output voltage swing [7]. Therefore, researchers are trying to achieve high DC gain by cascading or using multistage topologies operated at low bias current [8]. Fig. 1 shows the schematic of a two-stage CMOS opamp (in cascaded topology) [9], where each MOSFET is meant for accomplishing specific function. The MOSFETs M1 and M2 are used for differential gain acting as the input voltage to differential current converter. The M3 and M4 are acting as current mirror load used for recovering the differential current. The M5 is acting as the tail current and the M6 is acting as the voltage to current converter. Finally, M7 is the current sink load which is acting as the current to voltage converter. The opamp in Fig. 1 is an unbuffered amplifier which is characterised by its high output impedance [9].

In this two-stage opamp, the design parameters are mainly the size or aspect ratio (W/L) values of M1 through M8 and the current flowing through M5 and M7. This opamp topology segregates the gain and output voltage swing requirement where the first stage provides high gain, while the second stage gives large swings. Table I shows the desired specifications of the opamp taken from different sources [9]–[12]. From the desired specifications, the W/L of the MOSFETs have been evaluated through extensive DC simulations [13]–[15] in Cadence-spectre by employing the ratio of transconductance to current consumption (g_m/I_d) methodology [14]–[17]. Table II shows the sizing (W/L) summary of the MOSFETs constituting the opamp. Keeping the same W/L of the MOSFETs [Table II], the opamp topology [Fig. 1] can be simulated at the transistor level by using the ultra-thin-body silicon-on-insulator (UTBSOI) MOSFETs, as demonstrated in [13], [14]. Fig. 2 shows the UTBSOI based opamp (UTBSOI-opamp) that can be simulated by utilizing the BSIM-IMG model [18].
The mathematical definition of circuit sensitivity is [20]:

\[ S^y_x = \frac{\Delta y}{\Delta x} \mid \frac{x}{y} \]  

where \( S^y_x \) is the sensitivity, \( x \) is the changing parameter of the circuit’s component, and \( y \) is the circuit’s function (or performance parameter). Suppose, the parameter \( x \) is the \( W/L \) of the constituent MOSFETs in an amplifier IC, and it is crucial if the circuit sensitivity with respect to change in this parameter is very large. In other words, the variation in circuit’s function is large due to the change in the parameter \( x \). It plays a dominant role in ascertaining the crucial parameters of a component. Since the design of a circuit must be carried out by choosing as many cheap components as possible without degrading the desired specifications, so it is necessary to decide which components are crucial and how much is the required value of tolerance of its parameters.

In this paper, sensitivity of the performance parameters such as DC gain, CMRR, phase margin (PM), and unity-gain bandwidth (UGB) have been analyzed with respect to the perturbation in the \( W/L \) of MOSFETs (\( M_1, M_2, M_6, \) and \( M_7 \)) for the both two-stage CMOS and UTBSOI-opamp as shown in Fig. 1 and Fig. 2, respectively. Generally, due to the ageing of an IC, reliability issue like hot-carrier effect [21], [22] in the MOSFETs causes the generation of interface and oxide-trapped charges [23], [24], which in turn reduces the effective channel length of the MOSFETs. This is one of the reason why sensitivity analysis of the opamp as the function of perturbation in \( W/L \) of its constituent MOSFETs has been carried out in this paper. The channel lengths (\( L \)) of the selected MOSFETs have been changed accordingly to set \( \pm 10, \pm 20\% \) tolerances in perturbations of the \( W/L \) values.

II. UTBSOI MOSFETs

For more than four decades, the semiconductor industries are able to provide continuous support for improvement in the performance of electronic systems due to the invention of the MOSFETs. The prediction proclaimed by Moore’s law has been achieved through scaling down the MOSFETs. But for the last two decades, the scaling of bulk MOSFETs could not be continued at the same rate as predicted by Moore’s law because of several limitations like physical challenges, material challenges, technological challenges, etc [25]. The channel length (\( L \)) is one of the most important parameters of the MOSFETs which is defined as the distance between source and drain. Scaling down the \( L \) degrades the transconductance of the bulk MOSFETs, the subthreshold slope (\( SS \)) [26] degrades, and the threshold voltage (\( V_{th} \)) decreases. Due to these phenomena, the device can not be turned off easily even if the gate-to-source voltage (\( V_{gs} \)) [27] is lowered below the \( V_{th} \). It also causes leakage current due to the \( V_{th} \) reduction. These shortfalls observed in the bulk MOSFETs are collectively known as short-channel effects (SCE) [28]. Due to SCEs, characteristics of the bulk MOSFETs become increasingly sensitive to the \( L \) reduction. In addition to this, the process variation parameters of the bulk MOSFETs have become a major cause in degrading the performance of an IC. Different advanced architectures of MOSFETs [27], [29] have been put forward in the literature to overcome the limitations caused by SCEs. Out of those architectures, the dual-gated UTBSOI MOSFET as shown in Fig. 3 is the promising one [30].

The UTBSOI MOSFETs are grown over the SOI substrates with extremely uniform silicon films. The silicon substrate can be used as a back gate to bias the body [Fig. 3] provided that the thickness of the buried oxide (BO) is reduced [31]. Through this back gate bias, a flexibility of multiple \( V_{th} \) control can be achieved in the UTBSOI [30]. Moreover, the UTBSOI MOSFET has better scalability and superior controllability of gates over the shorter channel region [14] which...
increases the transconductance of the device. Analog, digital, or mixed signal circuits are always carefully verified through the circuit simulators, where compact models are used which represent the characteristics or conditions in the device in the form of (a) an equation, (b) an equivalent circuit, and (c) a table, together with the proper reasoning and assumptions [32]. Compact models for the semiconductor devices are very much essential for all types of electronic design and are the fundamental part of a Process-Design Kit (PDK) for a particular technology node. The PDKs consist of a set of technology definitions used to validate an IC from its desired specifications before being reproduced in silicon hardware. BSIM3 was selected as the world’s first industry-standard model for the MOSFET by Compact Model Coalition (CMC) in the year 1997, and it is in the production level PDKs especially for 180 nm technology node (BSIM3v3) [27]. The BSIM-IMG [18] is an industry-standard compact model targeted for the UTBSOI MOSFETs which is under standardization by the CMC. However, the post-layout of simulation UTBSOI based circuits is not possible till date due to the non-availability of PDK in the present simulators like Cadence-spectre [33].

III. RESULTS AND DISCUSSION

The W/L values of the constituent MOSFETs M1, M2, M6, and M7 have been chosen as the target components to study the variation in the performance parameters of the CMOS- and UTBSOI-opamps. The mentioned MOSFETs are chosen because these play a pivotal role in deciding the overall performance of the opamps unlike the other MOSFETs. The MOSFET pair M1 and M2 (M1,2) contributes more to the noise and other performance parameter variation over the M3, M4, and M5. Since resistance is a passive element and it is hard to implement in an IC [34], due to which the MOSFET pair M5 and M4 (M5,4) are used as the load resistance in the opamp. Thus, W/L of M5,4 pair are not considered. The M7 mirrors the I_rref through it. So, change in the W/L of M5 does not contribute to the variation of the performance parameters. The MOSFETs M6 and M7 forms the second stage of the opamp acting as the voltage to current converter [9]. Thus, consideration of W/L of these MOSFETs (M1,2, M6, and M7) are necessary in this analysis. The method of calculating the L value for −20% tolerance in perturbation of W/L of the M1,2 has been illustrated in Example 1.

Example 1. Referring to the Table II, $W_{12} = 4.37 \, \mu m$ and $L_{12} = 0.880 \, \mu m$. The initial aspect ratio $x_i$ is calculated as:

$$x_i = \frac{W_{12}}{L_{12}} = \frac{4.37 \, \mu m}{0.880 \, \mu m},$$

$$= 4.9659.$$  

The following relation yields the −20% tolerance in $W/L$ of $M_{1,2}$:

$$\frac{\Delta x}{x_i} \times 100 = -20\%.$$  

Using the value of $x_i$ obtained from (2) in (3) will yield $\Delta x = -0.99318$. The final value of aspect ratio $x_f$ is calculated as:

$$x_f = x_i - 0.99318,$$

$$= 3.9727.$$  

Equation (4) implies:

$$\frac{W}{L_{12f}} = 3.9727,$$

which will give the final value of $L_{12f} = 1.10 \, \mu m$.

Table III shows the calculated values of $L$ to achieve the required tolerances in perturbation of $W/L$ for the selected set of MOSFETs. However, in order to set 10% and 20% tolerances in perturbation of $W/L$ of $M_6$, the calculated values of $L_6$ are 178 nm and 163 nm respectively, which does not satisfy for the 180 nm technology. Therefore, these values have not been considered in this analysis (illustrated in Table VI and Table VII).

A summary of the simulation results of the opamps [13] are listed in Table IV. To observe the impact of the parasitic capacitance and resistance present in the CMOS-opamp, the layout is designed as shown in Fig. 4, where the open-loop and unity-gain configurations of the opamp are simulated accordingly. Some deviations have been observed between the pre- and post-layout simulation results, and the errors are listed in Table V. The reason for the errors is related to the inaccuracies associated with the parasitic components present.
in the layout. The $C_c$ (=1 pF) present in the CMOS-opamp is hard to include in the layout design since it requires large channel length and width which exceeds 30 µm for a metal insulator metal capacitor (mimcap). That is why, the $C_c$ has been connected outside the circuit. The area of the CMOS-opamp extracted from the layout design is $1.569 \times 10^{-3}$ mm$^2$.

The performance parameters observed for different values of tolerances of perturbation in $W/L$ of $M_{1,2}$, $M_6$, and $M_7$ are given in Table VI (shown at the next page). The sensitivity of DC gain, CMRR, PM, and UGB with respect to the perturbation in $W/L$ of the MOSFETs is computed in the MATLAB encoded through Algorithm 1. Table VII shows the sensitivity values of the UTBSOI-opamp obtained in this analysis. The same can also be obtained for the CMOS-opamp using the Algorithm 1.

Comparison charts showing the sensitivity of UTBSOI-opamp in terms of DC gain, CMRR, PM, and UGB are shown in Fig. 5. In the UTBSOI-opamp, the DC gain is least sensitive towards the perturbation in $W/L$ of $M_{1,2}$ [Fig. 5(a)]. A large DC gain sensitivity ($\sim$3.1249) [Table VII] is observed for the 10% tolerance of perturbation in $W/L$ of $M_6$ [Fig. 5(a)]. This also implies that the $W/L$ of $M_6$ can be changed accordingly in order to increase the DC gain. The CMRR is more sensitive towards the perturbation in $W/L$ of $M_{1,2}$ and least towards that of $M_7$ [Fig. 5(b)]. The PM is more sensitive towards the perturbation in $W/L$ of $M_7$ [Fig. 5(c)] and UGB is more sensitive towards the perturbation in $W/L$ of $M_6$ [Fig. 5(d)]. The same goes for the sensitivity analysis performed over

\textbf{Algorithm 1: Algorithm to compute the sensitivity.}

\textbf{Require:} $W$, $L$, $L_f$, $y[i]$, $y_{new}[i]$

\textbf{Ensure:} Sensitivity values ($S$) of DC gain, CMRR, PM, and UGB.

\begin{itemize}
  \item $W \rightarrow$ Channel width, $l \rightarrow$ Initial channel length [Table II]
  \item $L_f \rightarrow$ Final channel lengths [Table III]
  \item $y \rightarrow$ Initial performance parameters [Table IV]
  \item $y_{new} \rightarrow$ Final performance parameters [Table VI]
\end{itemize}

\begin{algorithm}
1: \textbf{Start}
2: \textbf{repeat}
3: \hspace{0.5cm} $x \leftarrow W/l$
4: \hspace{0.5cm} $i \leftarrow 1$
5: \hspace{0.5cm} \textbf{while} $i \leq \text{LENGTH}(L_f)$ \textbf{do}
6: \hspace{1cm} $x_{new}[i] \leftarrow W/L_f[i]$
7: \hspace{1cm} $\Delta x[i] \leftarrow x_{new}[i] - x$ \{Perturbation in aspect-ratio of MOSFETs\}
8: \hspace{1cm} $\Delta y[i] \leftarrow y_{new}[i] - y$
9: \hspace{1cm} $S[i] \leftarrow \{x/y \times (\Delta y[i]/\Delta x[i])\}$
10: \hspace{0.5cm} end while
11: \hspace{0.5cm} until Sensitivity values ($S$) of DC gain, CMRR, PM, and UGB are obtained.
\end{algorithm}

\begin{table}[h]
\centering
\caption{SUMMARY OF PRE- AND POST- LAYOUT SIMULATION RESULTS OF CMOS-opamp.}
\begin{tabular}{|c|c|c|c|}
\hline
\textbf{Specifications} & \textbf{Pre-layout results} & \textbf{Post-layout results} & \textbf{Error (%)} \\
\hline
& (as given in Table IV) & & \\
\hline
UGB (MHz) & 19.0 & 18.98 & 0.10 \\
PM (°) & 54.5 & 55.02 & 0.95 \\
DC gain (dB) & 72.8 & 73.57 & 1.05 \\
CMRR (dB) & 93.4 & 77.73 & 16.78 \\
Power (mW) & 0.189 & 0.188 & 0.529 \\
Area (mm$^2$) & - & 1.569$\times 10^{-3}$ & - \\
\hline
\end{tabular}
\textbf{The minus sign (−) signifies the decrease in performance parameter in post-layout simulation.}
\end{table}

\begin{table}[h]
\centering
\caption{Sensitivity values of DC gain, CMRR, PM, and UGB of the UTBSOI-opamp with respect to the tolerances of perturbation in $W/L$ of the selected MOSFETs.}
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline
\textbf{Perturbation in $W/L$ of $M_{1,2}$} & \textbf{Performance parameters} & \textbf{UTBSOI-opamp} & \textbf{Error (%)} \\
& & $-20\%$ & $-10\%$ & $10\%$ & $20\%$ \\
\hline
DC gain (dB) & 0.0008 & 0.0360 & 0.0283 & 0.0665 \\
CMRR (dB) & 0.2382 & 0.2516 & 0.3021 & 0.3818 \\
PM (°) & 0.0783 & 0.1014 & 0.1323 & 0.1687 \\
UGB (MHz) & 0.2147 & 0.2052 & 0.3669 & 0.4059 \\
\hline
\textbf{Perturbation in $W/L$ of $M_6$} & \textbf{Performance parameters} & \textbf{UTBSOI-opamp} & \textbf{Error (%)} \\
& & $-20\%$ & $-10\%$ & $10\%$ & $20\%$ \\
\hline
DC gain (dB) & 2.8474 & 3.2489 & - & - \\
CMRR (dB) & 0.2174 & 0.2257 & - & - \\
PM (°) & 0.9600 & 1.2549 & - & - \\
UGB (MHz) & 1.4391 & 1.9484 & - & - \\
\hline
\textbf{Perturbation in $W/L$ of $M_7$} & \textbf{Performance parameters} & \textbf{UTBSOI-opamp} & \textbf{Error (%)} \\
& & $-20\%$ & $-10\%$ & $10\%$ & $20\%$ \\
\hline
DC gain (dB) & 0.8186 & 0.9731 & 1.8149 & 1.9612 \\
CMRR (dB) & 0.0170 & 0.0197 & 0.0243 & 0.0446 \\
PM (°) & 0.7975 & 0.9390 & 0.9894 & 0.5821 \\
UGB (MHz) & 1.6282 & 1.6230 & 2.1856 & 1.4938 \\
\hline
\end{tabular}
\textbf{Tolerance (%) in perturbation of $W/L$: $-20\%$, $-10\%$, 10\%, 20\%}
\end{table}
the sensitivity of the performance parameters of the opamps as the function of the perturbation in W/L values of the constituent MOSFETs. From the sensitivity analysis, it is concluded that the W/L of M6 is the crucial parameter for deciding the DC gain and PM. The UGB and CMRR are more sensitive towards the W/L of M7 and M1,2 respectively. The sensitivity observed in UTBSOI-opamp towards the perturbation of W/L of the constituent MOSFETs is higher than that of CMOS-opamp. Analytical modeling of the sensitivity of performance parameters of the opamps as the function of perturbation in W/L would be a welcome step towards the work presented in this paper.

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